

Title	Page	Title	Page	Title	Page
COVER PAGE	1	(RSVD)	41	(RSVD)	81
BLACK DIAGRAM	2	(RSVD)	42	(RSVD)	82
CPU_DISPLAY	3	DC IN CONN	43	(RSVD)	83
CPU_DDR_CHA	4	(RSVD)	44	(RSVD)	84
CPU_DDR_CHB	5	RT6575D_5V_A/3D3V_A	45	(RSVD)	85
CPU_LPSS/ISH_I2C	6	NCP81206MN_CPU_VCORE(1/3)	46	(RSVD)	86
CPU_POWER1	7	NCP81206MN_CPU_VCORE(2/3)	47	(RSVD)	87
CPU_POWER2	8	NCP81206MN_CPU_VCORE(3/3)	48	DUMMY PARTS	88
PCH_POWER1	9	(RSVD)	49	SCREW HOLE/EMI CAP	89
CPU_POWER CAP1	10	NCP81253MN_1V_VCCSA	50	(RSVD)	90
CPU_POWER CAP2	11	VDDQ/VT/2D5V_S3	51	(RSVD)	91
DDR4-SODIMM1	12	ID0V_S5/1V_VCCST/1V_VCCIO	52	(RSVD)	92
DDR4-SODIMM2	13	G9661_1D8V_S5	53	(RSVD)	93
CPU_STRAP	14	(RSVD)	54	(RSVD)	94
CPU_PCIE/SATA/USB3/USB2	15	LCD CONN	55	(RSVD)	95
CPU_CLOCK	16	(RSVD)	56	(RSVD)	96
CPU_AUDIO/SDIO/SDXC	17	HDMI LEVEL SHIFTER/CONN	57	(RSVD)	97
CPU_LPC/SPI/SMBUS/CLINK	18	RTD2136 eDP to LVDS	58	CLOCK	98
CPU_CS-2/EMMC	19		59	XDP	99
CPU_POWER MANAGEMENT	20	HDD	60	TABLE OF CONTENT	100
CPU_VSS	21	(RSVD)	61	CHANGE HISTORY	101
CPU_JTAG/MISC	22	PWR BTN/SIDE KEY/LED	62	POWER SEQUENCING	102
CPU_RSVD/CFG	23	SSD_KEY.M	63	POWER BLOCK DIAGRAM	103
SIO_IT8772E	24	(RSVD)	64	SMBUS BLOCK DIAGRAM	104
SPI/RTC	25	(RSVD)	65	THERMAL/AUDIO BLOCK DIAGRAM	105
(RSVD)	26	NGFF_WLAN	66		
AUDIO_ALC269	27	(RSVD)	67		
(RSVD)	28	DEBUG HEADER	68		
Audio Jack/SPK CONN	29	(RSVD)	69		
(RSVD)	30	(RSVD)	70		
LAN_RTL8111H	31	(RSVD)	71		
RJ45+TRANSFORMER	32	(RSVD)	72		
SD/CR_RTSS170	33	(RSVD)	73		
USB2 CONN	34	(RSVD)	74		
USB3 CONN	35	(RSVD)	75		
(RSVD)	36	(RSVD)	76		
(RSVD)	37	(RSVD)	77		
CAMERA CONN	38	(RSVD)	78		
(RSVD)	39	(RSVD)	79		
POWER SEQUENCING	40	(RSVD)	80		

# Eiffel215i-KBLU Schematics Document

R :None Installed  
DBG :Debug  
O :OCP Option.  
NONOCP:Non OCP  
SD: USB Card reader  
SDSOC:internal card reader  
CAM :Camera

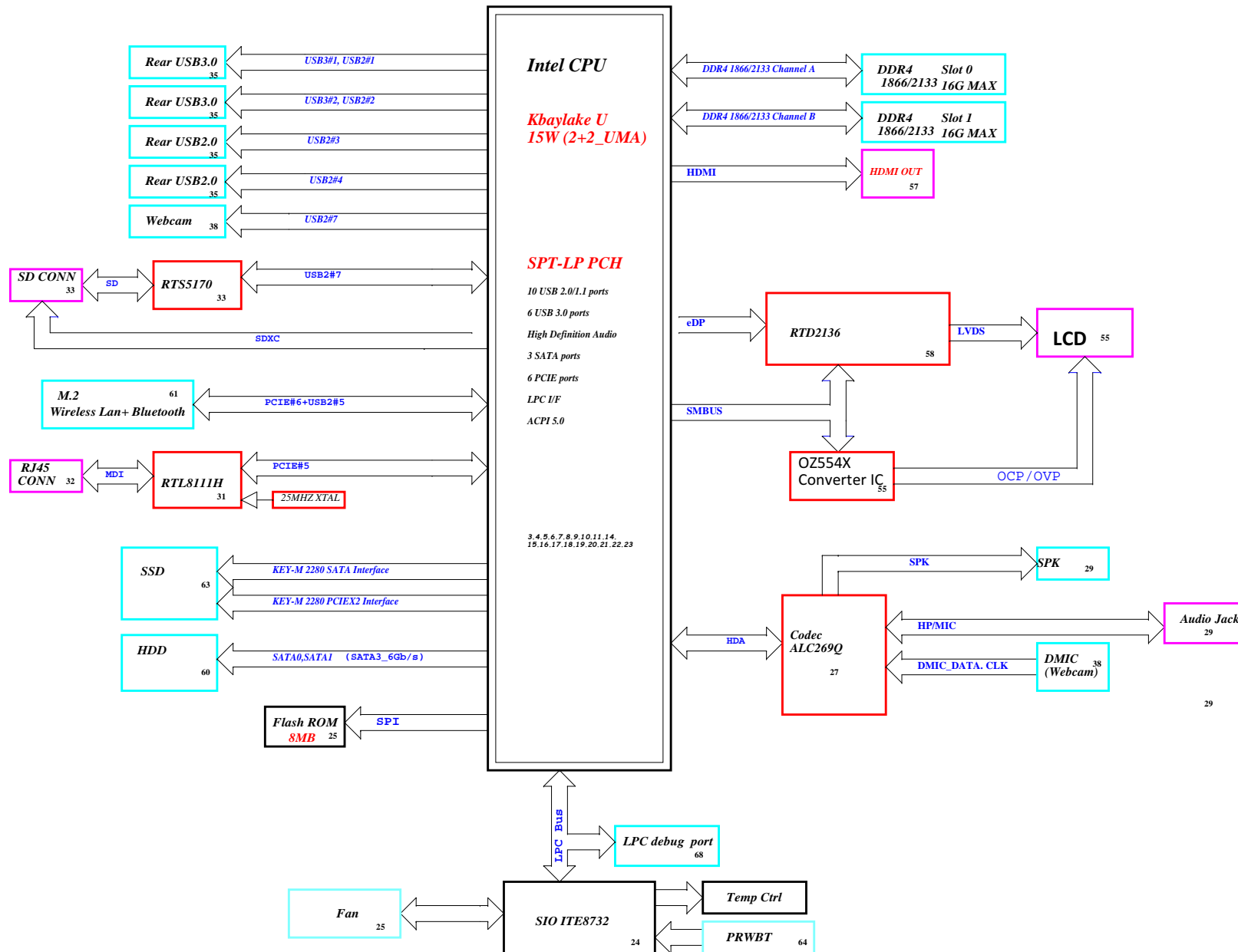
Project code :3PD090010001  
PCB No :16557  
Revision :-1  
Project Name :Eiffel215i  
Size :225\*12mm

# Eiffel215i\_KBLU Block Diagram

Project code : 3PD090010001  
 PCB No : 16557  
 Revision : -1  
 Project Name :Eiffel215i\_KBL\_U

## PCB LAYER

L1:Top  
 L2:VCC  
 L3:Signal  
 L4:Signal  
 L5:GND  
 L6:Signal



## 56.2 Skylake-U and Kaby Lake-U Package and Ball Compatibility

Skylake-U and Kaby Lake-U (2+2 & 2+3e) are intended to be package and ball compatible, so the same Kaby Lake system designs can be used for both.

Reference Design CPU: KBL-U  
 I/O: Bristol238i-SKL-U

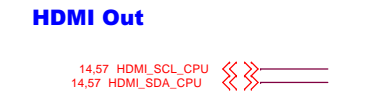
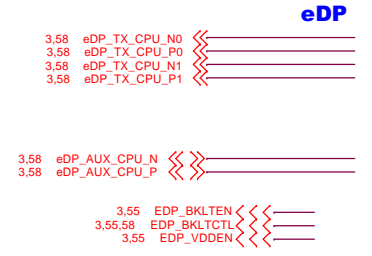
- For Internal IO Connect
- For Internal IC
- For external Rear IO Connect
- For external DB Side IO Connect
- For external DB Side IO Connect

<Core Design>

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 Taipei Hsien 221, Taiwan, R.O.C.

Block Diagram		
Size C	Document Number	Rev
	Eiffel215i-KBL_U	-1
Date: Saturday, May 06, 2017	Sheet 2 of 105	

Main Func = CPU



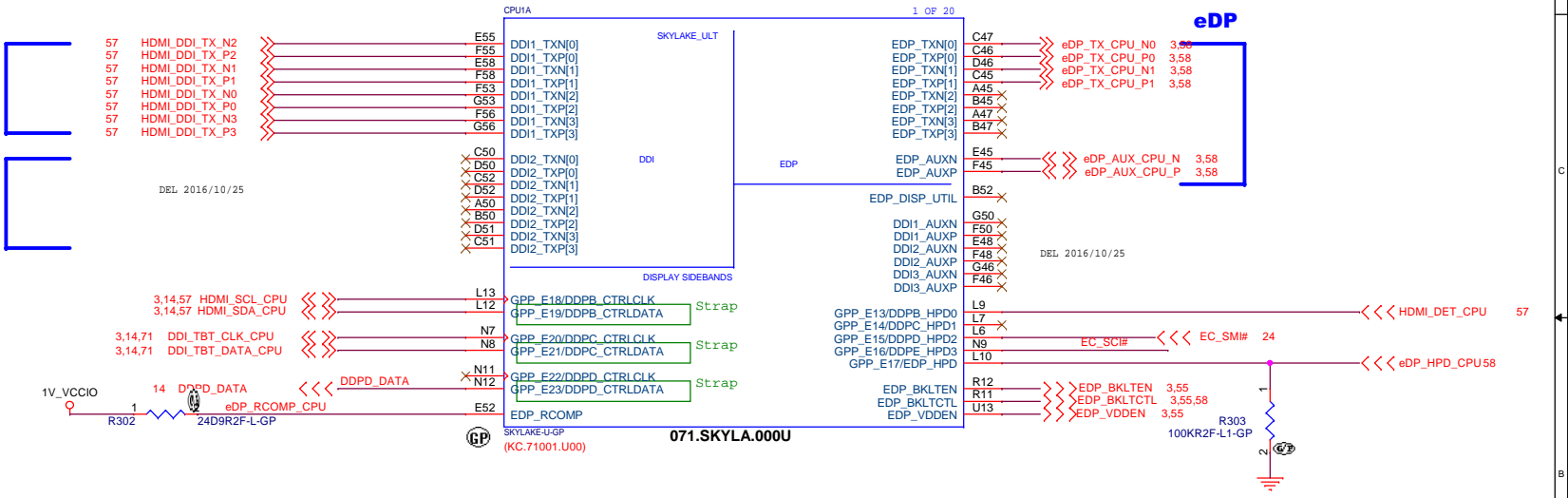
HDMI Out

Thunderbolt

(#543016) eDP\_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω ±1%	Max = 100 mils

Design Guideline:  
Skylake processor signal eDP\_RCOMP should be connected to the VCCIO rail via a single 24.9 ±1% Ω resistor.



<Core Design>

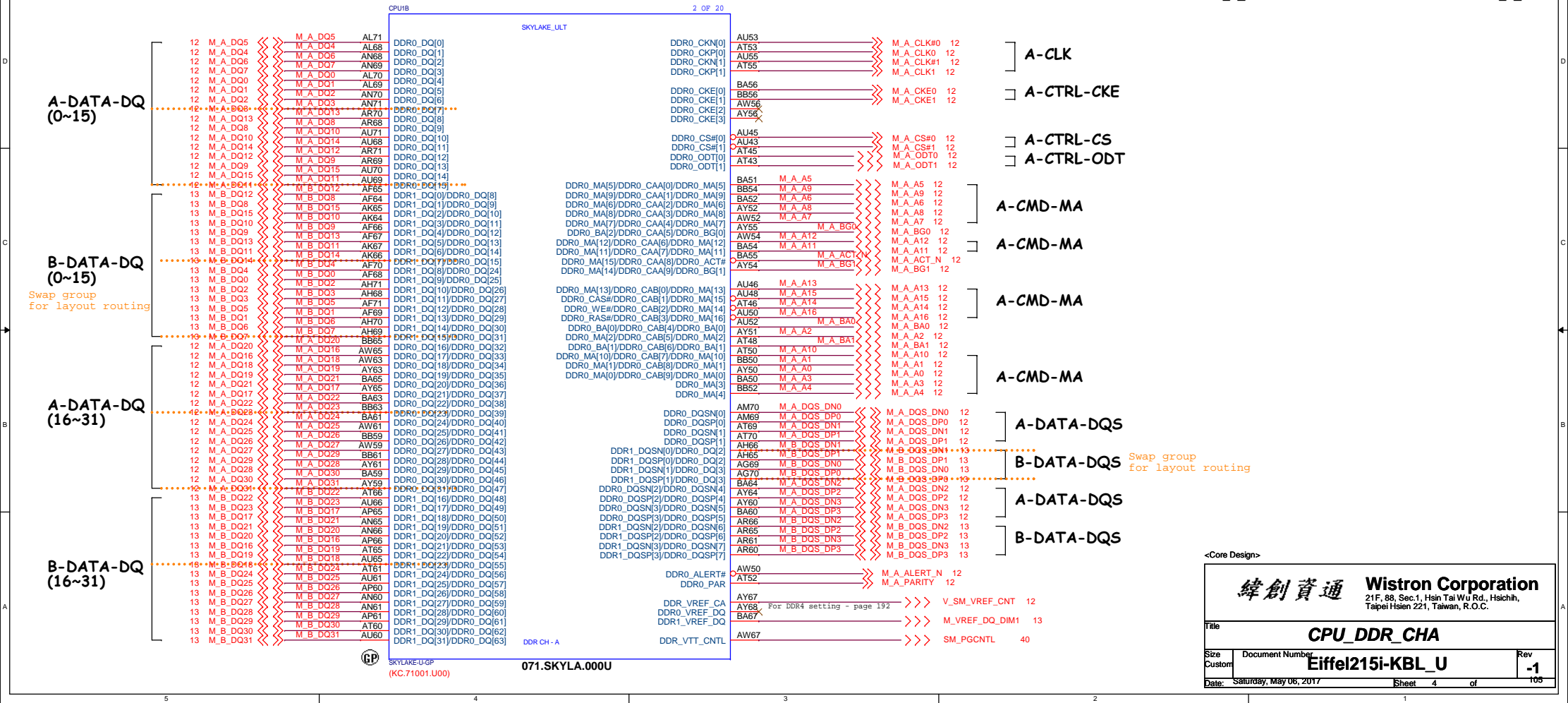
**緯創資通**

**Wistron Corporation**

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Title		
CPU_DISPLAY		
Size	Document Number	Rev
Custom	Eiffel215i-KBL_U	-1
Date:	Saturday, May 06, 2017	Sheet 3 of 105

DDR4 ball type: Interleaved Type



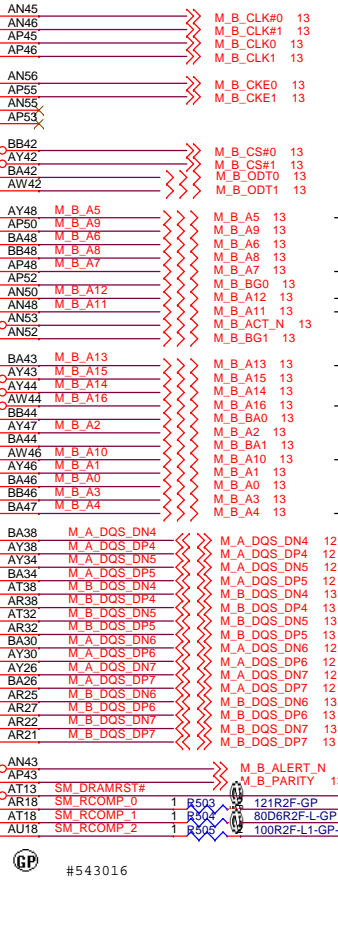
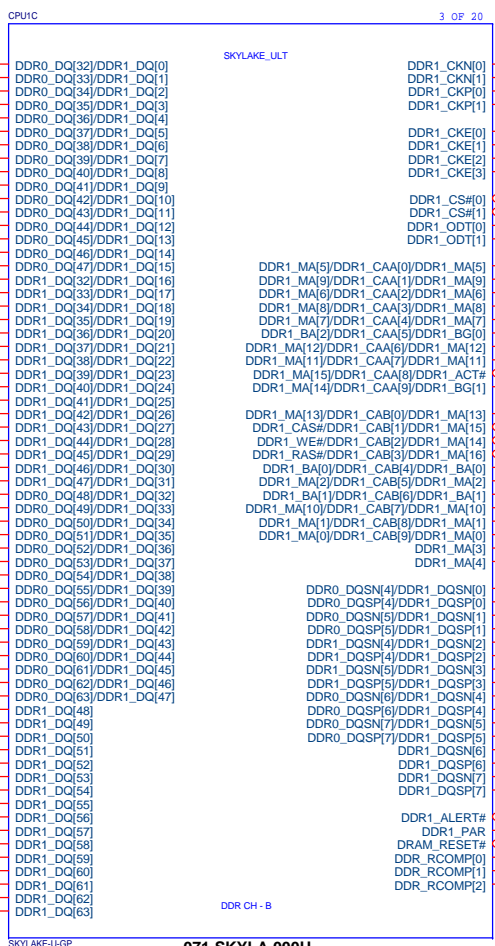
Main Func = CPU

A-DATA-DQ  
(32~47)

B-DATA-DQ  
(32~47)

A-DATA-DQ  
(48~63)

B-DATA-DQ  
(48~63)



B-CLK

B-CTRL-CKE

B-CTRL-CS

B-CTRL-ODT

B-CMD-MA

B-CMD-MA

B-CMD-MA

A-DATA-DQS

B-DATA-DQS

A-DATA-DQS

B-DATA-DQS

SM\_DRAMRST#\_R12,13,89

1D2V\_S3

R501 470R2F-GP

20140922

R502 1 2 0R0402-PAD-2-GP

SB add back EC501 SC22P50V2JN-4GP

<Core Design>

緯創資通 Wistron Corporation

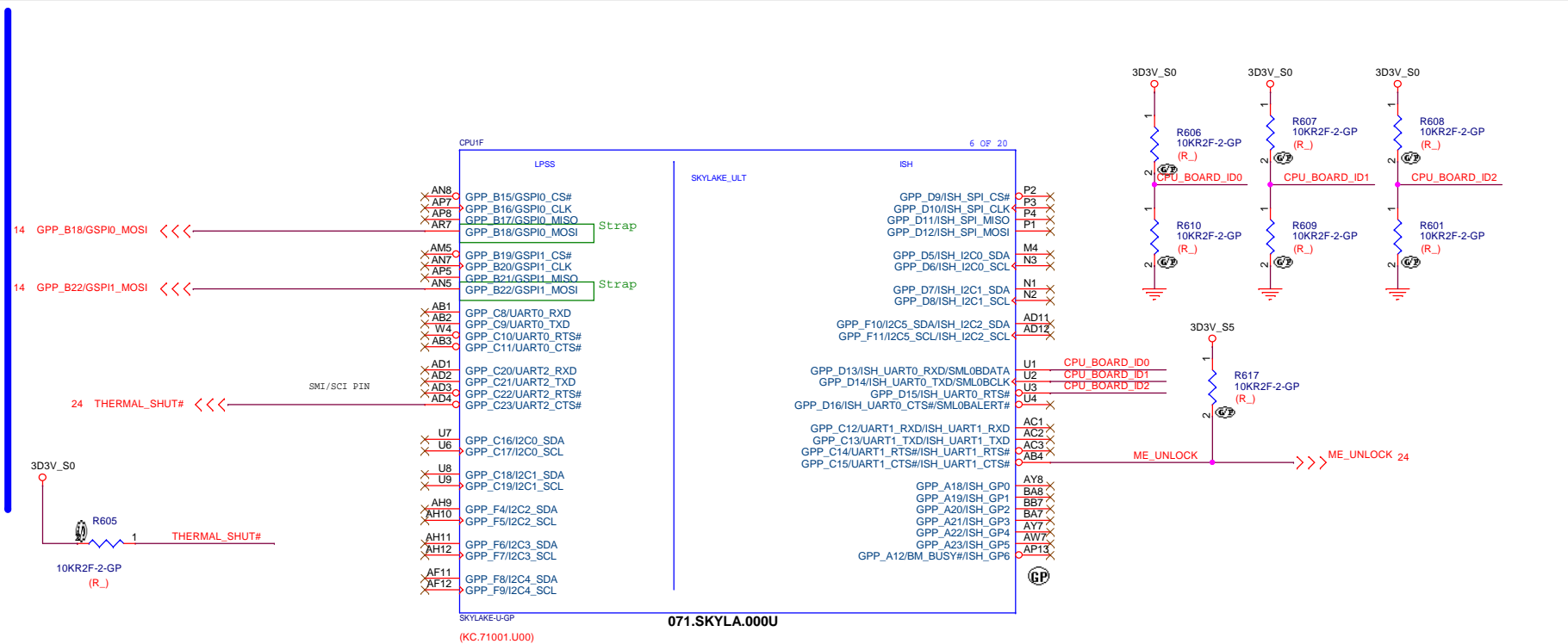
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.

Title CPU\_DDR\_CHB

Size Custom Document Number Eiffel215i-KBL\_U Rev -1

Date: Saturday, May 06, 2017 Sheet 5 of 105

Main Func = PCH



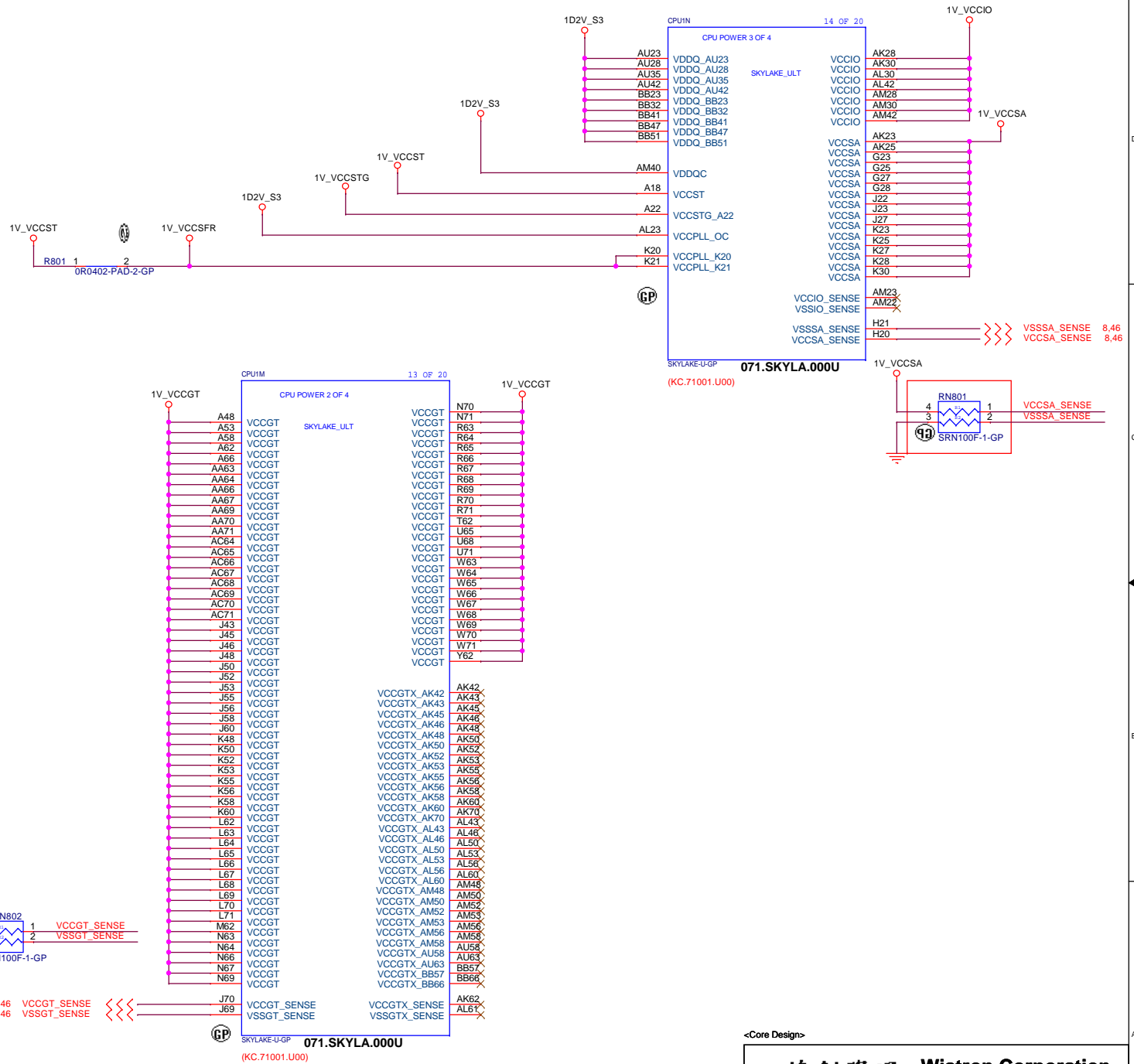
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<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>CPU_LPSS/ISH_I2C</b>			
Size	Document Number	Rev	
Custom		<b>-1</b>	
Date: Saturday, May 06, 2017		Sheet	6 of 105





## Main Func = CPU



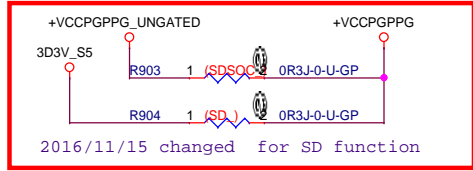
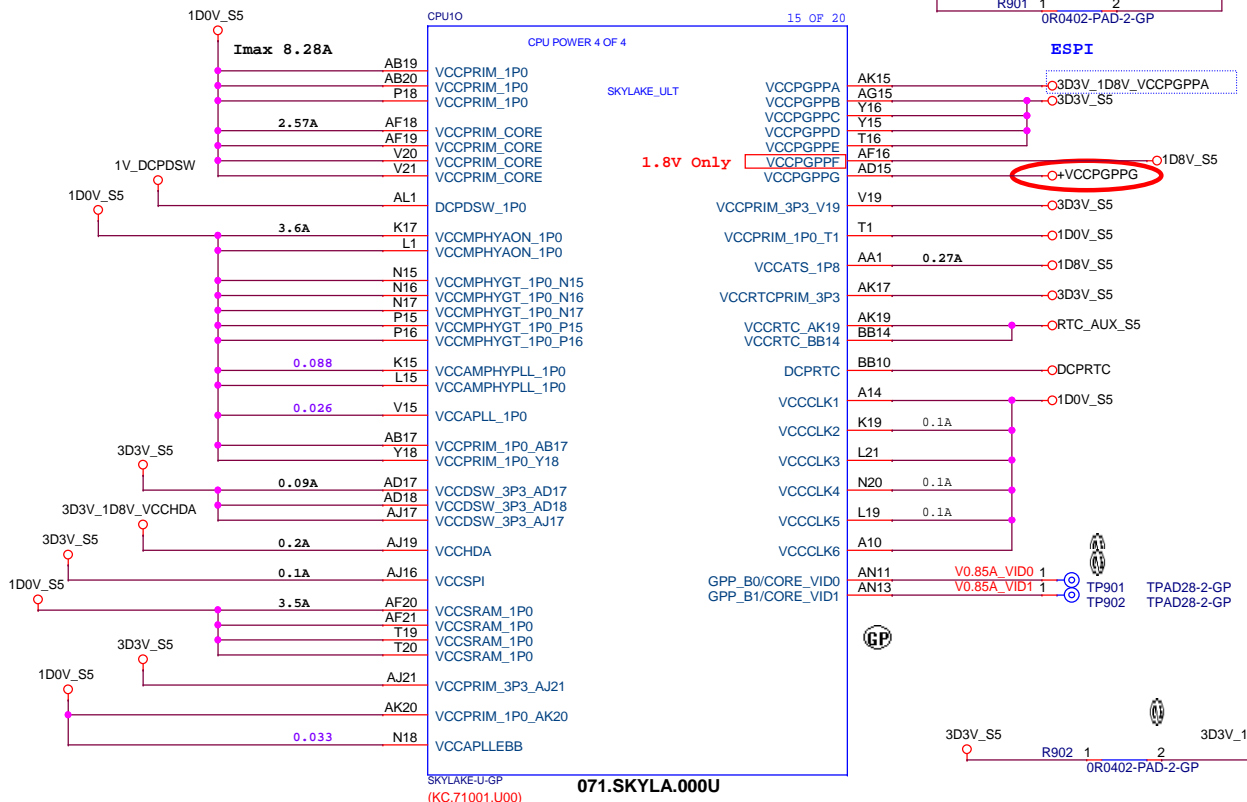
### <Core Design>

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Title				<b>CPU_POWER1</b>			
Size	Document Number					Rev	
A3	<b>Eiffel215i-KBL_U</b>					<b>-1</b>	
Date:	Saturday, May 06, 2017			Sheet	8	of	105



Main Func = PCH



eSPI\_508740:

Table 2: eSPI/LPC Pinlist for SKL-PCH

SKL-PCH Pin Name	Direction	LPC Signal	eSPI Signal	Pin Description
GPP_A_0	in	RCINB	<GPIO>	
GPP_A_1	inout	LAD_0	ESPI_IO_[0]	LPC Cmd/Addr/Data or eSPI Data [0]
GPP_A_2	inout	LAD_1	ESPI_IO_[1]	LPC Cmd/Addr/Data or eSPI Data [1]
GPP_A_3	inout	LAD_2	ESPI_IO_[2]	LPC Cmd/Addr/Data or eSPI Data [2]
GPP_A_4	inout	LAD_3	ESPI_IO_[3]	LPC Cmd/Addr/Data or eSPI Data [3]
GPP_A_5	out	LFRAMEB	ESPI_CSB	LPC Frame or eSPI Chip Select
GPP_A_6	inout	SERIRQ	<GPIO>	
GPP_A_7	iod	PIRQAB	<GPIO>	
GPP_A_9	out	LPC_CLKOUT_0	ESPI_CLK	
GPP_A_14	out	SUS_STATB	ESPI_RESETB	
GPP_C_5_SM LOALERTB	input	ESPI_EN Pin Strap		eSPI Enable Pin Strap; sampled at RMSRST# deassertion 0: LPC; 1: eSPI
VCCPGPPA	-	3.3V	1.8V	Voltage for all GPIOs in GPP_A group

NOTE: All pin mappings are subject to change. Refer to the SKL-PCH EDS for final pin list.

<Core Design>

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Title

CPU\_(POWER1)

Size Custom

Document Number

Eiffel215i-KBL\_U

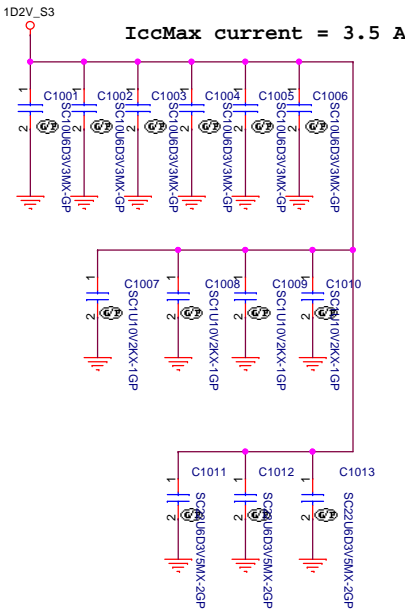
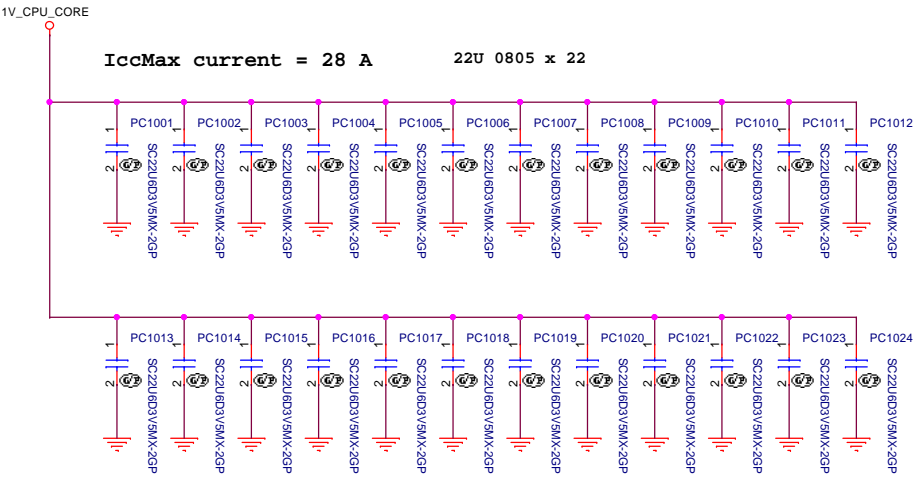
Rev

-1

Date: Saturday, May 06, 2017

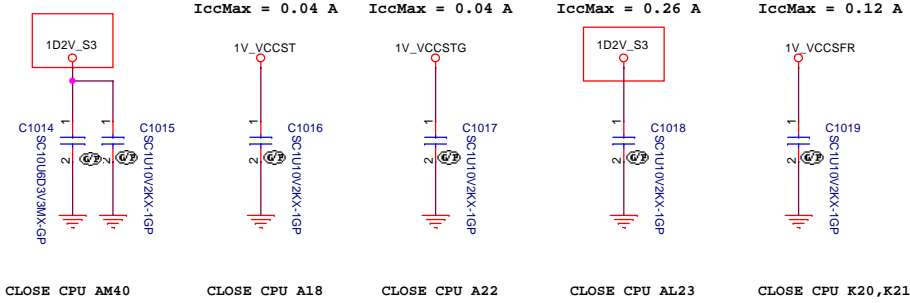
Sheet 9 of 105

Main Func = CPU



U22 15W	IA	750MHz	33A (28A)	23A (21A)	2.1mΩ (2.35mΩ)	30A (TBD)	200mv/30us	1X0.15uH	2X330uF/9mW	30X22uF
								Or	1x330uF/9mW	36x22uF
	GT	750KHz	40A (31A)	18A (18A)	3.1mΩ	38A (TBD)	70mv/10us	1X0.15uH	2X330uF/9mW	24X22uF
								Or	1x330uF/9mW	36x22uF
	SA	750KHz	6A (5A)	6A (4A)	10.3mΩ	4A (TBD)	200mv/30us	1X0.42uH	None	5X22uF

VDDQ	2x 10 uF 0402 (Placeholder)		Place on secondary side, underneath the package
	4x 1 uF 0201 (Placeholder)		
		4x 10 uF 0402	Place as close to the package as possible
		3 x 22 uF 0603	Place as close to the package as possible



CLOSE CPU AM40    CLOSE CPU A18    CLOSE CPU A22    CLOSE CPU AL23    CLOSE CPU K20,K21

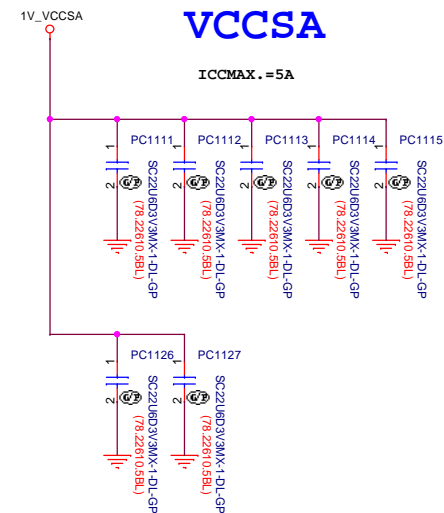
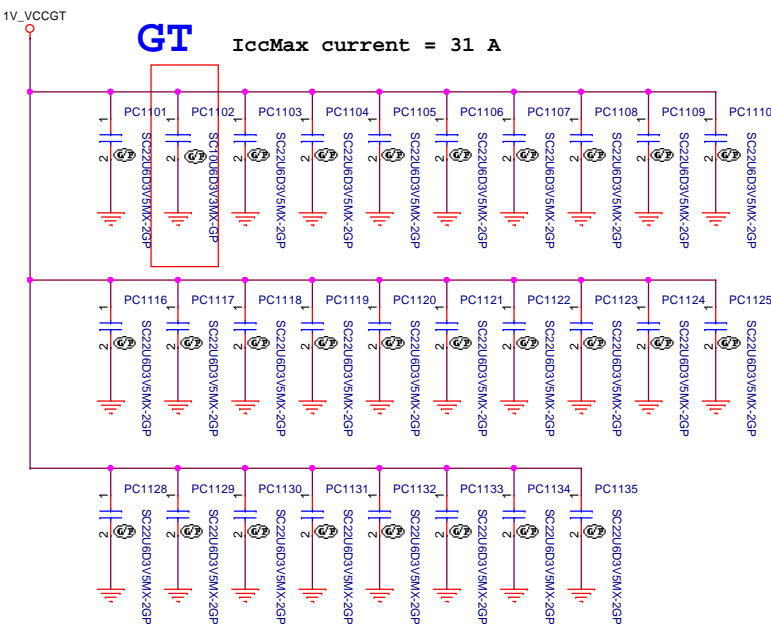
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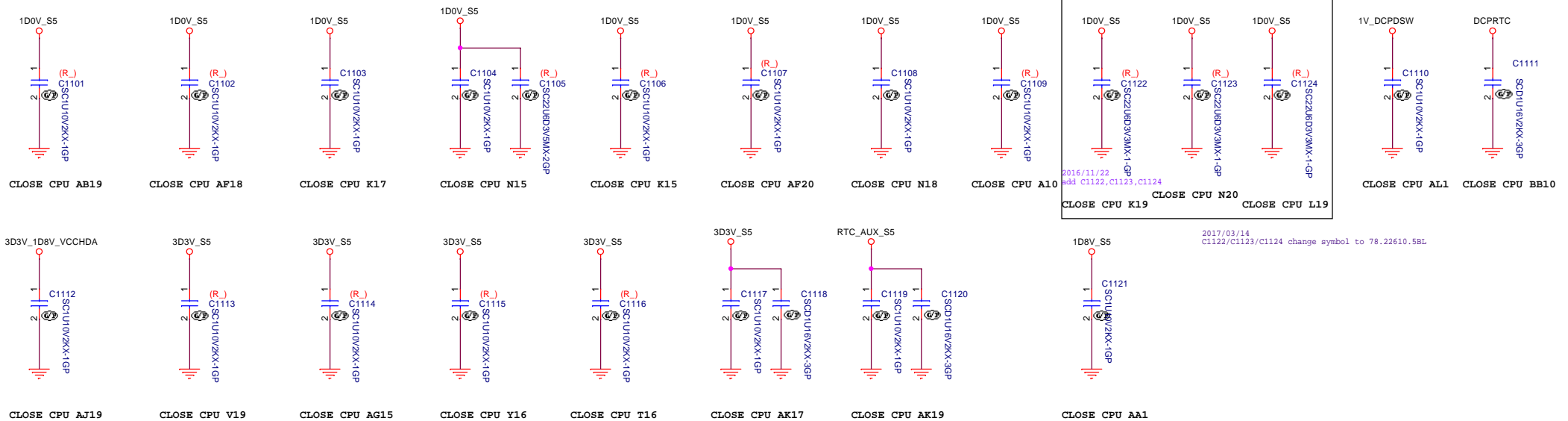
Title CPU\_POWER CAP1

Size A3 Document Number Eiffel215i-KBL\_U Rev -1

Date: Saturday, May 06, 2017 Sheet 10 of 105



U22 15W	IA	750MHz	33A (28A)	23A (21A)	2.1mΩ (2.35mΩ)	30A (TBD)	200mv/30us	1X0.15uH	2X330uF/9mW	30X22uF
								Or	1x330uF/9mW	36x22uF
	GT	750KHz	40A(31A)	18A (18A)	3.1mΩ	38A (TBD)	70mv/10us	1X0.15uH	2X330uF/9mW	24X22uF
								Or	1x330uF/9mW	36x22uF
	SA	750KHz	6A (5A)	6A (4A)	10.3mΩ	4A (TBD)	200mv/30us	1X0.42uH	None	5X22uF



**<Core Design>**

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Tapei Hsien 221, Taiwan, R.O.C.

Title	<b>CPU_POWER CAP2</b>
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Size A3	Document Number <b>Eiffel215i-KBL_U</b>	Rev <b>-1</b>
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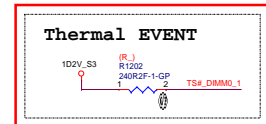
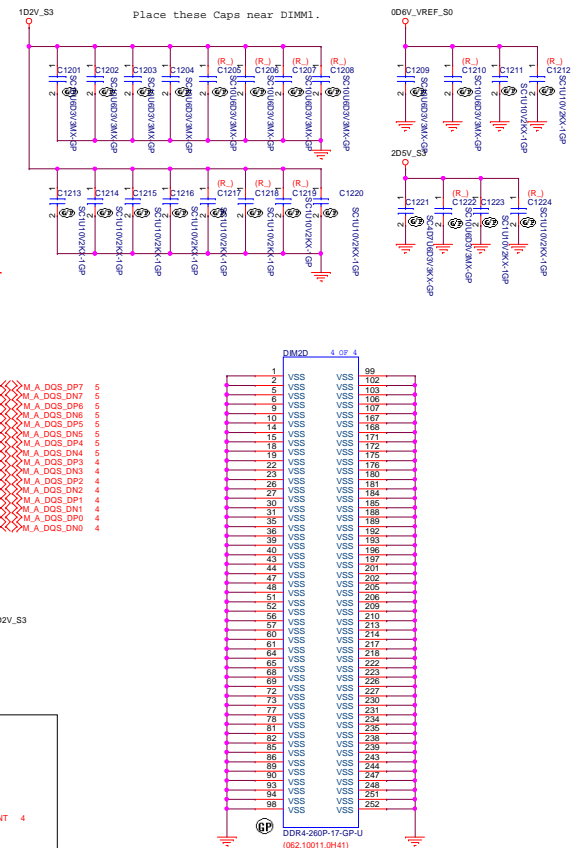
Date: Saturday, May 06, 2017 Sheet 11 of 105

## Standard Type

**Note:**  
SA0\_DIM0 = 0, SA1\_DIM0 = 0  
SO-DIMMA SPD Address is 0xA0  
SO-DIMMA TS Address is 0x30

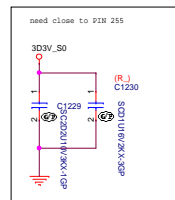
**Layout Note:**

Place these Caps near DIMM1.

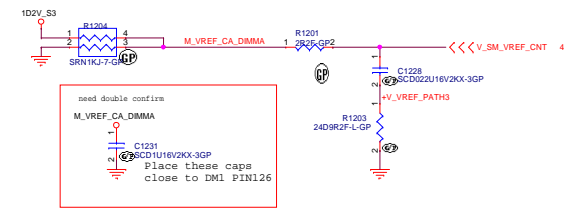


**SPD Address of XMM1**

<b>SPD SA1</b>	<b>0</b>
<b>SPD SA0</b>	<b>0</b>



## SA\_DIMM\_VREFDQ



**<Core Design>**

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**DDR4-SODIMM1**

Size

Document Number	Eiffel215i-KBL U
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Date: Saturday, May 06, 2017

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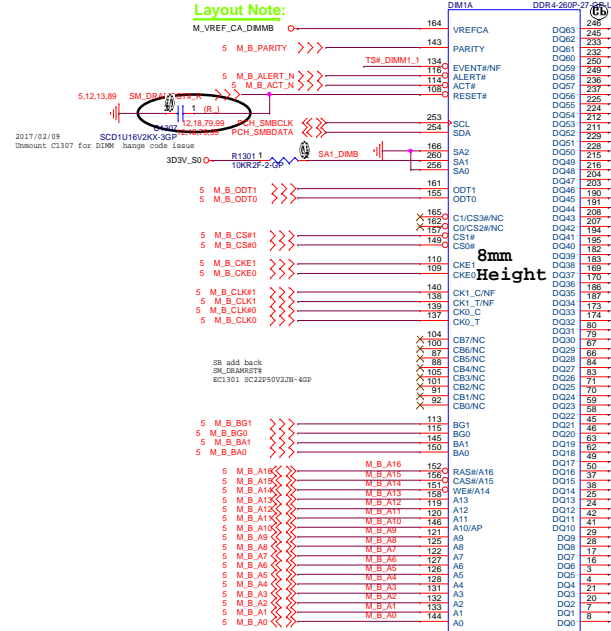
# Main Func = DDR SODIMM

## Reverse Type

Note:  
SO-DIMMB SPD Address is 0xA4  
SO-DIMMB TS Address is 0x34

All VREF traces should  
have width=20mil;  
spacings 20 mil

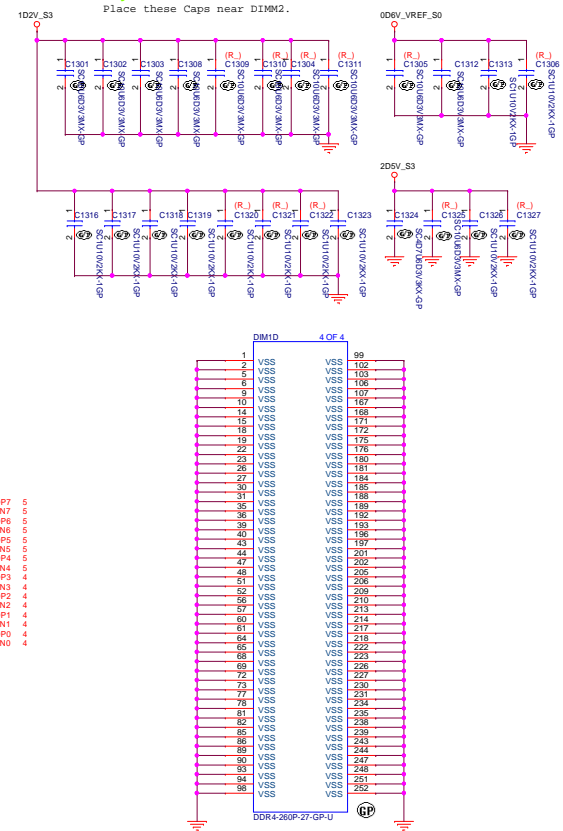
### Layout Note:



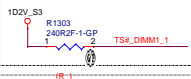
8mm  
Height

### Layout Note:

Place these Caps near DIMM2.



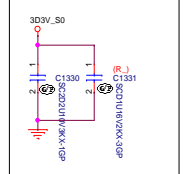
### Thermal EVENT



### SPD Address of XMM1

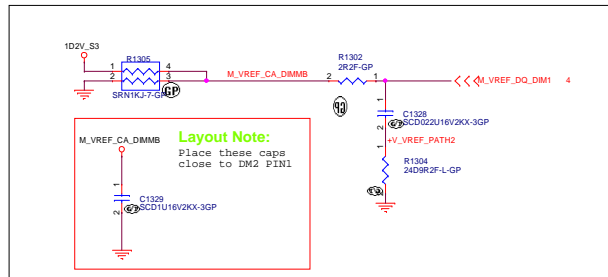
SPD SA1	1
SPD SA0	0

need close to PIN 255



### Layout Note:

Place these caps  
close to DM2 PIN1



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File	DDR4-SODIMM2		
Size	Document Number	Eiffel215-KBL_U	Rev
A2			-1
Date	Saturday, May 06, 2017	Sheet	13 of 106

SSID = STRAP

STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC  
SHOULD BE PLACED OUTSIDE KOZ AREA

Description	Display Port B Detected	Display Port C Detected	Reserved	No reboot	Boot BIOS strap bit BBS	Flash descriptor security override	Display Port D Detected
GPIO	GPP_E19	GPP_E21	SPI0_MISO	GPP_B18	GPP_B22	HDA_SDO	GPP_E23
Schematic							
High	Detected	Detected		Enable	LPC	Disable	Detected
Low	Not Detected	Not Detected		Disable	SPI	Enable	Not Detected
	internal pull-down	internal pull-down	internal pull-up	internal pull-down	internal pull-down	internal pull-down	internal pull-down

Description	Top Swap Override	Reserved	Reserved	Reserved	TLS Confidentiality	eSPI or LPC	Reserved
GPIO	GPP_B14	SPI0_MOSI	SPI0_IO2	SPI0_IO3	GPP_C2	GPP_C5	GPP_B23
Schematic							
High	Enable				Enable	eSPI	
Low	Disable				Disable	LPC	
	internal pull-down	internal pull-up	internal pull-up	internal pull-up	internal pull-down	internal pull-down	internal pull-down

<Core Design>

**WEBCAM**



Timing diagram for SRN1KJ-7GP (R.) showing signals: USB0, USBVSEN, SATAGP0, SATA\_LED0, HPGP\_M2\_SATA\_DET0, USB\_OC#0, USB\_OC#1, USB\_OC#2. The diagram shows signal transitions over time with markers for 1230 Simon, 123025, and 123030. Key events include SRN1KJ-7GP (R.) and SRN1KJ-3-GP.

16	PCIe #12	SATA #2	Intel PCIe Storage Device #3
15	PCIe #11	SATA #1	
14	PCIe #10	GbE	Intel PCIe Storage Device #2
13	PCIe #9	GbE	
12	PCIe #8	SATA #1	Intel PCIe Storage Device #1
11	PCIe #7	SATA #0	
10	PCIe #6		
9	PCIe #5	GbE	
8	PCIe #4	GbE	
7	PCIe #3	GbE	
6	USB3 #6	PCIe #2	
5	USB3 #5	PCIe #1	
4	USB3 #4		
3	USB3 #3	SSIC #2	
2	USB3 #2	SSIC #1	
1	USB3 #1 (Capable of OTG)		

Table 27. Socket 2 Module Configuration

State #	Module Configuration Decodes				Module Type and Main Host Interface <sup>1</sup>	Port Configuration <sup>2</sup>
	CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)		
0	GND	GND	GND	GND	SSD – SATA	N/A
1	GND	N/C	GND	GND	SSD – PCIe	N/A



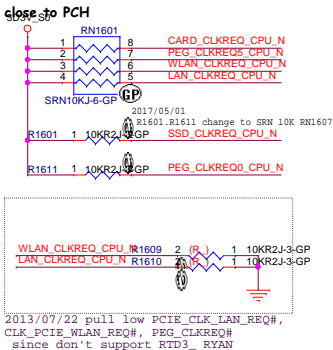
Main Func = PCH

SD4.0

LAN

WLAN

EC



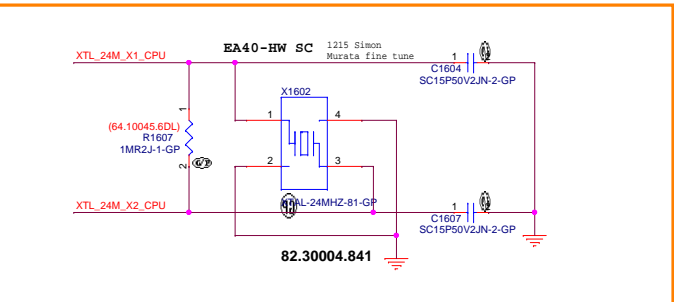
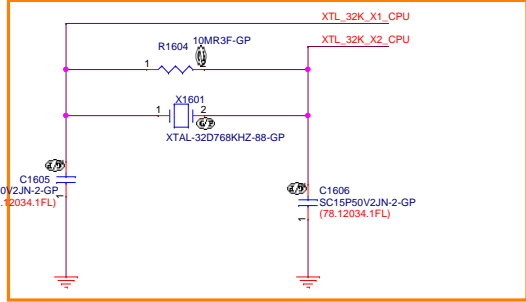
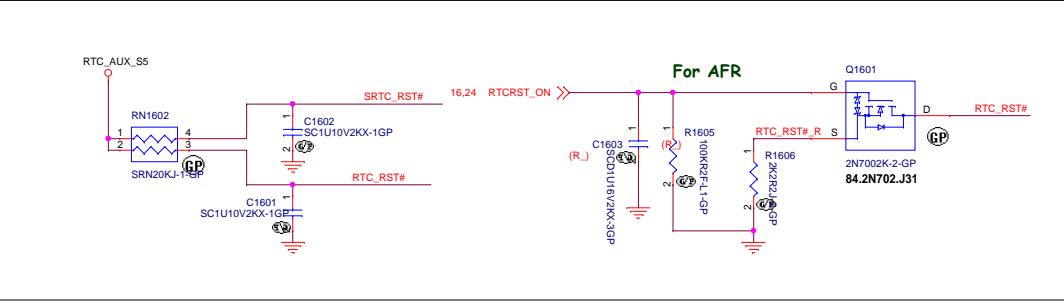
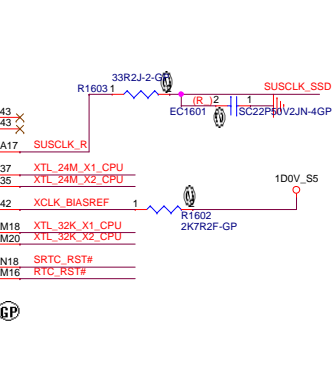
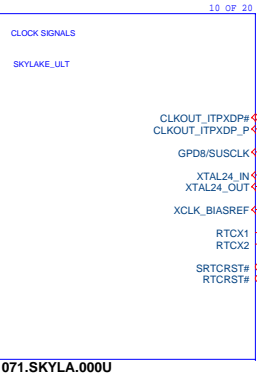
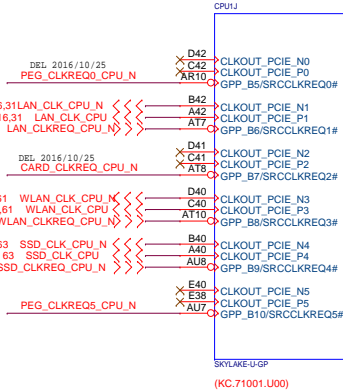
Thunderbolt

LAN

SDXC

WLAN

SSD



Main Func = PCH

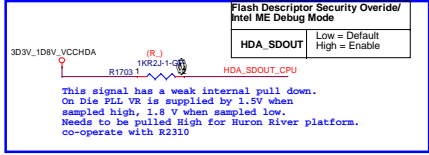
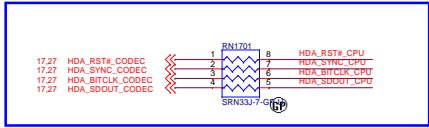
Audio Code

17.27 HDA\_RST#\_CODEC  
17.27 HDA\_SYNC\_CODEC  
17.27 HDA\_BITCLK\_CODEC  
17.27 HDA\_SDOUT\_CODEC  
17.27 HDA\_SDOIN\_CPU  
14.17.27 HDA\_SPKR

2017/03/14  
C1701 change symbol from 78\_48774\_1PF to 78\_48784\_1PF  
use the COMMON Part

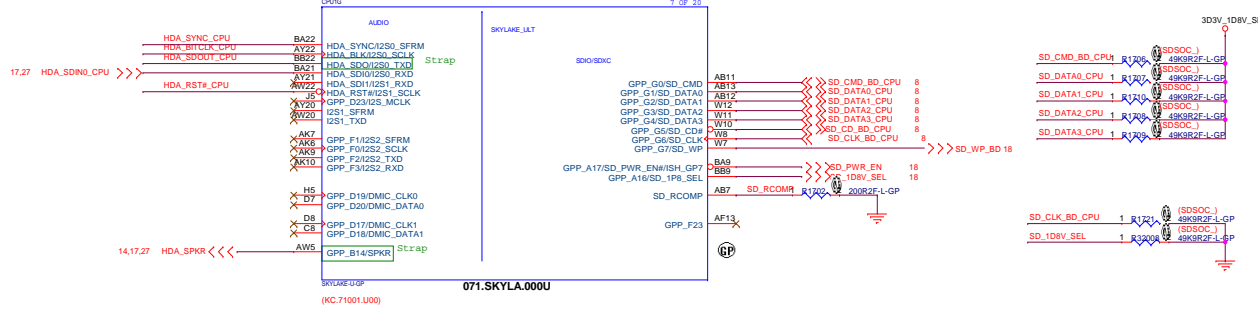


Michael 2011/01/16  
For EMI



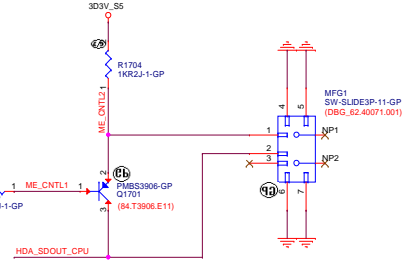
Flash Descriptor Security Override/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default High = Enable

This signal has a weak internal pull down.  
On Die PLL VR is supplied by 1.5V when  
sampled high, 1.8 V when sampled low.  
Needs to be pulled High for Huron River platform.  
co-operate with R2310



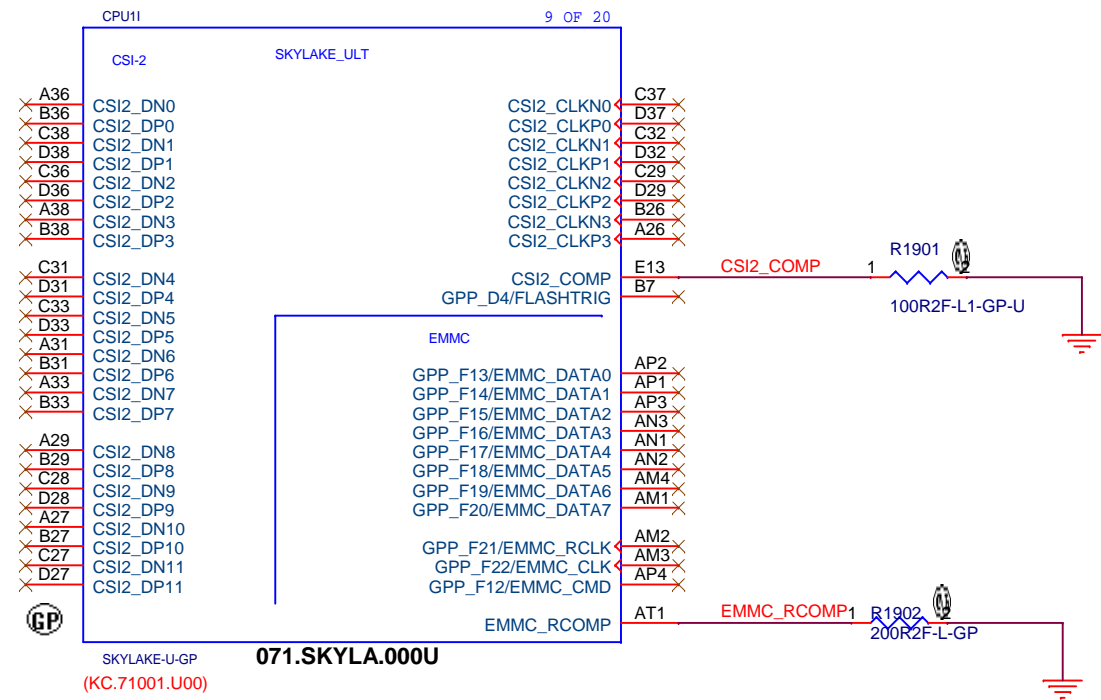
Flash Descriptor Security Override	
HDA_SDOUT	Low = Default High = Debug mode

- 17.24 ME\_UNLOCK <<< ME\_UNLOCK
- 1. Resume GPIO
- 2. Default High





Main Func = PCH



<Core Design>

緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**CPU\_CS-2/EMMC**

Size  
A4

Document Number

**Eiffel215i-KBL\_U**

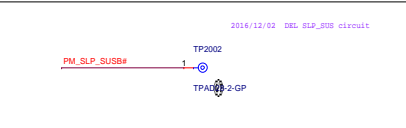
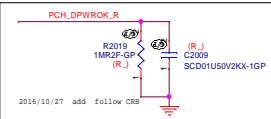
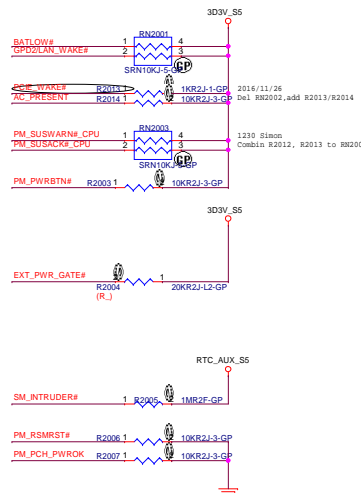
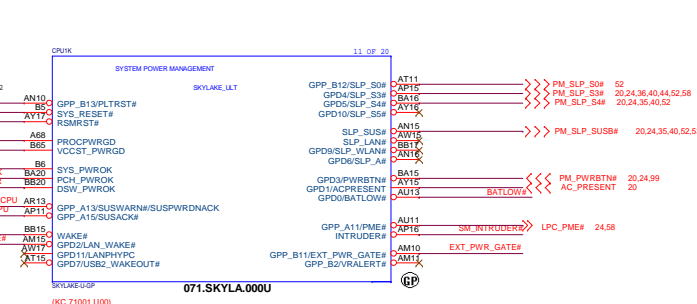
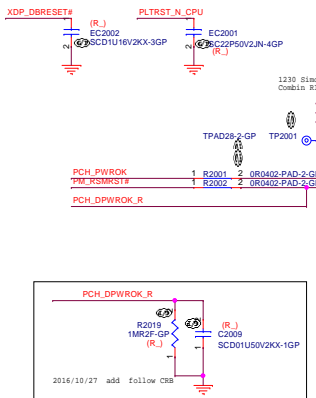
Rev  
**-1**

Date: Saturday, May 06, 2017

Sheet 19 of 105

Main Func = PCH

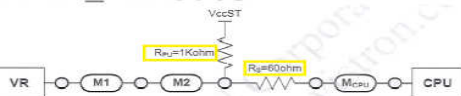
20,40,43,99 SYS\_PWROK >>>  
20,40 PCH\_PWROK >>>  
20,31,61 PCIE\_WAKE# >>>  
40 ALL\_SYS\_PWRGD >>>  
20,24,68,99 PLTRST\_N\_CPU <<<  
24 PCH\_DPWRROK\_R <<<  
  
20,24,36,40,44,52,58 PM\_SLP\_S3# <<<  
20,24,35,40,52 PM\_SLP\_S4# <<<  
20,24,99 PM\_PWRBTN# >>>  
20 AC\_PRESENT >>>  
  
20,40,99 VCCST\_PWRGD <<<  
  
40,89,99 PM\_RSMRST# <<<  
15,20,99 XDP\_DBRESET# >>>  
20GPD2LAN\_WAKE# >>>



#543016 Rev0.7  
1. VCCST\_PWRGD is only 1.0 V tolerant.  
2. VCCST\_PWRGD must go low during 8x pwr states, regardless of the voltage level of VCCST

VCCST\_PWRGD / HWM201:

VCCST\_PWRGOOD

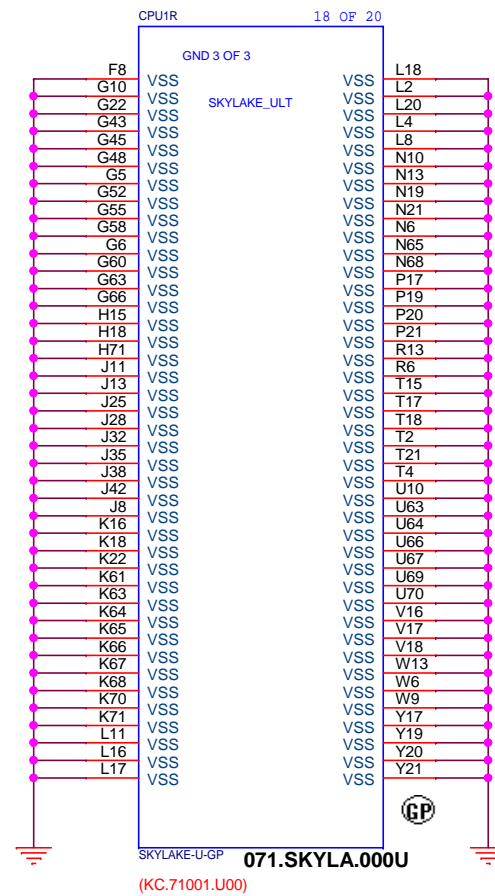
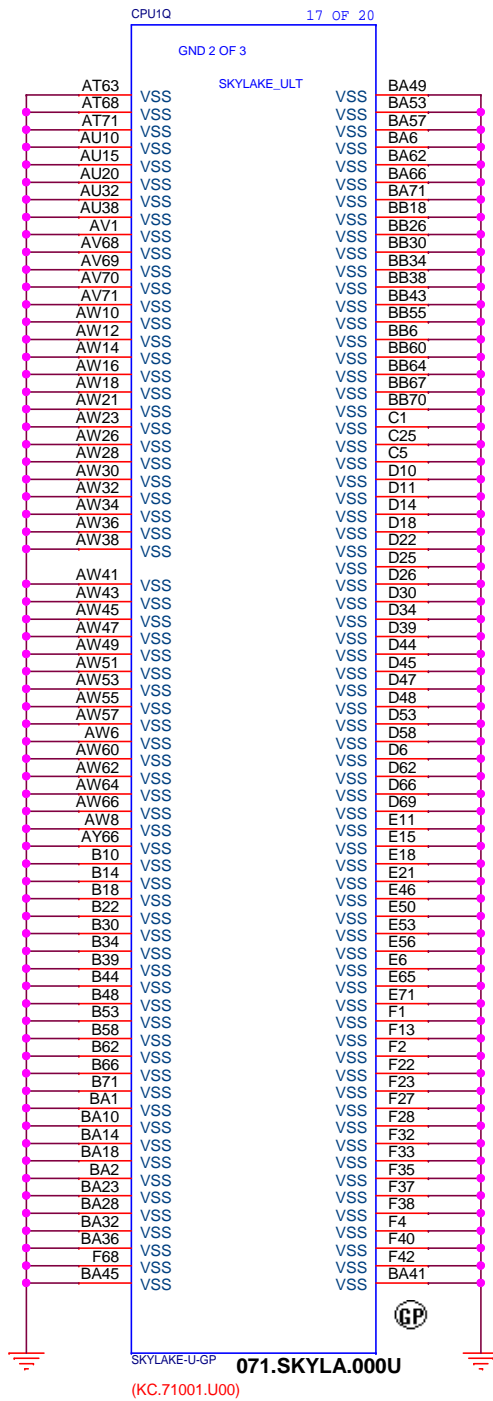
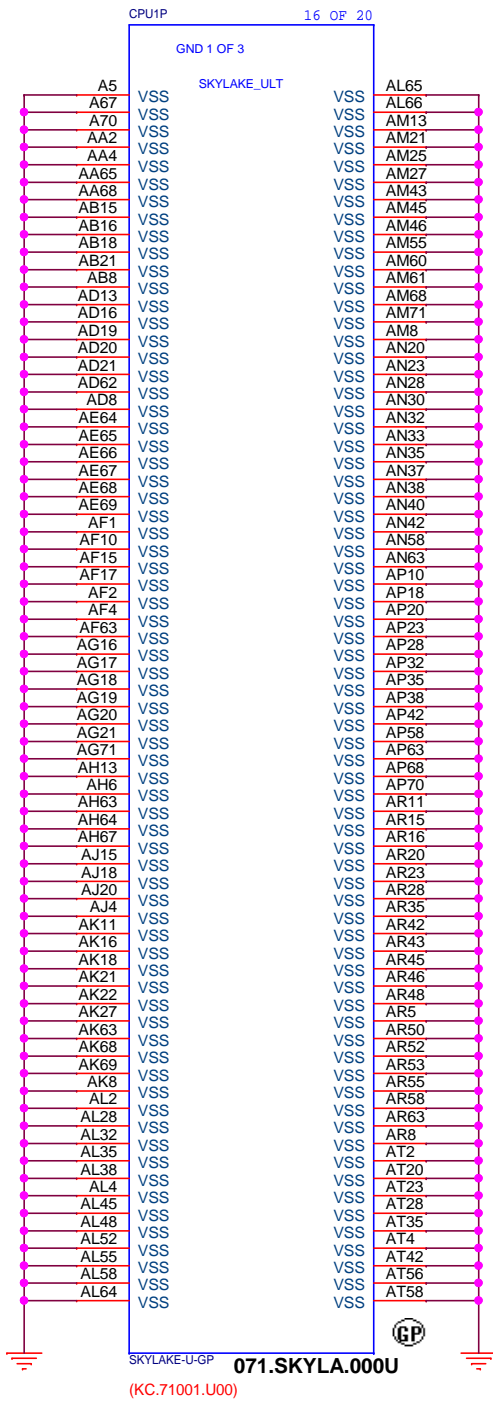


VCCST\_PWRGOOD is a signal on the processor that indicates both the VCCST power supply and VDDQ power supply are within voltage tolerance specification

GPP\_A13-15 pin(LPC/eSPI):

Name	Internal Pull-Up/ Pull-Down (Note 1)	De-Glitch (Note 2)		Multiplexed With	Default
		Input	Output		
GPP_A13	None	No	Yes	LPC mode: SUSWRN# / SUSPWRDNACK eSPI mode: None	SUSWRN# / SUSPWRDNACK (LPC mode) GPI (eSPI mode)
GPP_A14	None	No	Yes	LPC mode: SUS_STAT# eSPI mode: ESPI_RESET#	SUS_STAT# (LPC mode) ESPI_RESET# (eSPI mode)
GPP_A15	None	No	Yes	LPC mode: SUS_ACK# eSPI mode: None	SUS_ACK# (LPC mode) GPI (eSPI mode)

Main Func = PCH



<Core Design>

<b>緯創資通</b>			<b>Wistron Corporation</b>		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,			Taipei Hsien 221, Taiwan, R.O.C.		
Title					
<b>CPU_VSS</b>					
Size	Document Number				Rev
Custom	<b>Eiffel215i-KBL_U</b>				<b>-1</b>
Date:	Saturday, May 06, 2017		Sheet	21	of 105

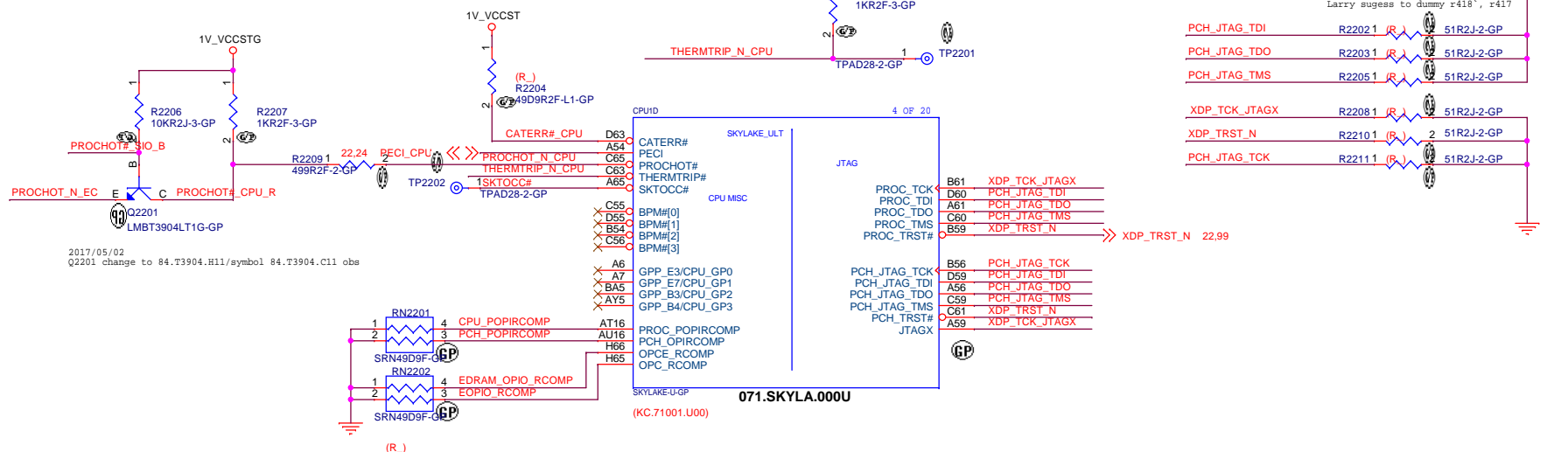
**Main Func = CPU**

22,24 PEGI\_CPU <>\_\_\_\_\_

由EC 端控制  
是否能改成 Touch\_slp#

24 PROCHOT\_N\_EC >> PROCHOT\_N\_EC

46 PROCHOT# CPU\_R &gt;&gt;\_\_\_\_\_



PROCHOT#	<b>Processor Hot:</b> PROCHOT# goes active when the processor temperature monitoring sensor(s) detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. This signal can also be driven to the processor to activate the TCC.	I/O	GTL I OD O	SE	All processor lines
THERMTRIP#	<b>Thermal Trip:</b> The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all executions when the junction temperature exceeds approximately 130 °C. This is signaled to the system by the THERMTRIP# pin. Refer to the appropriate platform design guide for termination requirements.	O	OD	SE	All processor lines

## <Core Design>

**緯創資通** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title	<b>CPU JTAG/MISC</b>
-------	----------------------

Size	Document Number	Rev
Custom	<b>Eiffel215i-KBL U</b>	<b>-1</b>
Date:	Saturday, May 06, 2017	Sheet 22 of 105



**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.

Intel recommends placing test points on the board for CFG pins.

- **CFG[0]:** Stall reset sequence after PCU PLL lock until de-asserted:
  - 1 = (Default) Normal Operation; No stall.
  - 0 = Stall.
- **CFG[1]:** Reserved configuration lane.
- **CFG[2]:** PCI Express\* Static x16 Lane Numbering Reversal.
  - 1 = Normal operation
  - 0 = Lane numbers reversed.
- **CFG[3]:** Reserved configuration lane.
- **CFG[4]:** eDP enable:
  - 1 = Disabled.
  - 0 = Enabled.
- **CFG[6:5]:** PCI Express\* Bifurcation
  - 00 = 1 x8, 2 x4 PCI Express\*
  - 01 = reserved
  - 10 = 2 x8 PCI Express\*
  - 11 = 1 x16 PCI Express\*
- **CFG[7]:** PEG Training:
  - 1 = (default) PEG Train immediately following RESET# de assertion.
  - 0 = PEG Wait for BIOS for training.
- **CFG[19:8]:** Reserved configuration lanes.

All processor lines.  
CFG[2], CFG[6:5] and  
CFG[7] are relevant  
for H and S-processor  
line only and test point  
may be placed on the  
board for them.

**Processor Select:** This pin is for compatibility with future platforms. It should be unconnected for SKL.

NA

All processor lines

**<Core Design>**

緯創資通

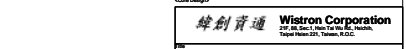
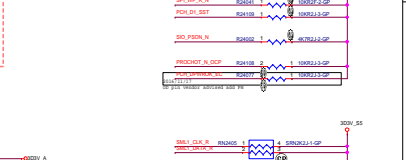
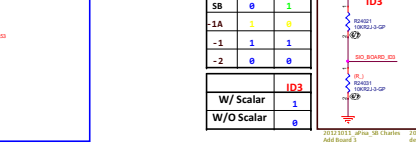
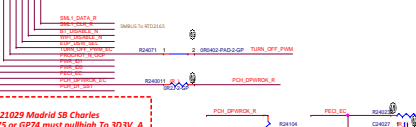
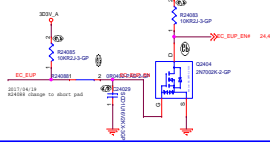
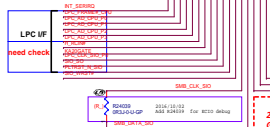
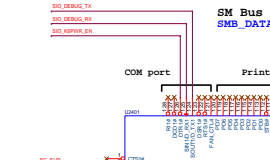
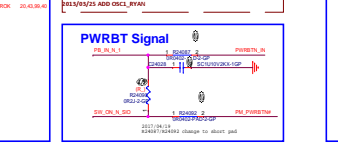
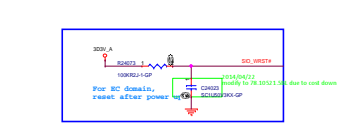
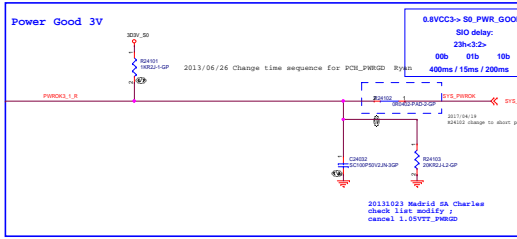
**Wistron Corporation**

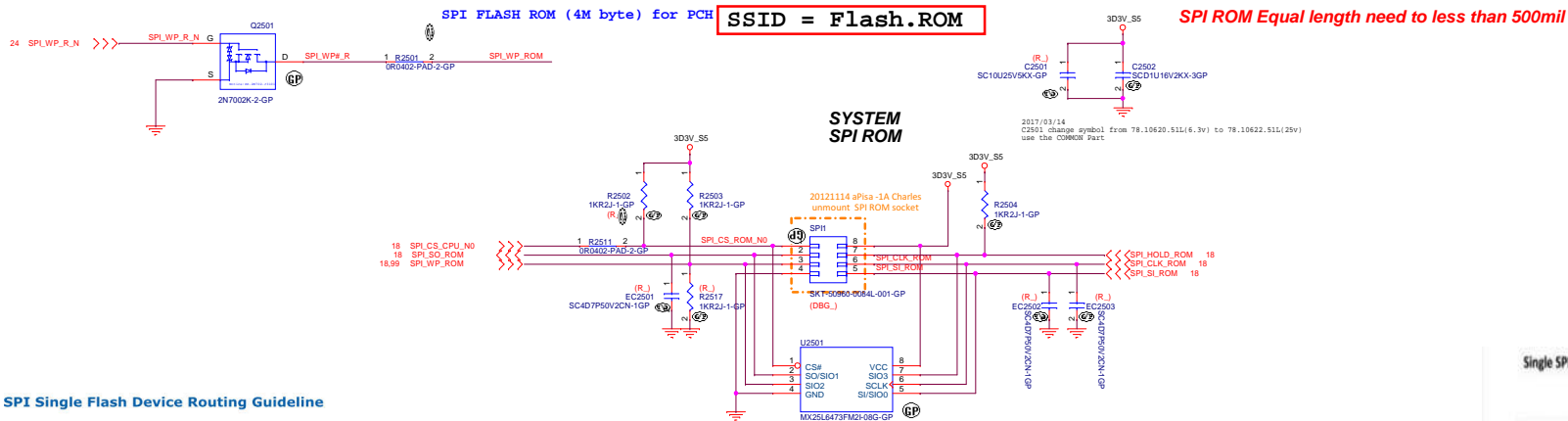
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title	<b>CPU RSVD/CFG</b>
-------	---------------------

Size Custom	Document Number <b>Eiffel215i-KBI II</b>	Rev <b>1</b>
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Date: Saturday, May 06, 2017 Sheet 23 of 105





### 25.2.1.1 SPI Single Flash Device Routing Guideline

Figure 25-2. SPI Single Flash Device Routing Guidelines for SPI Signals

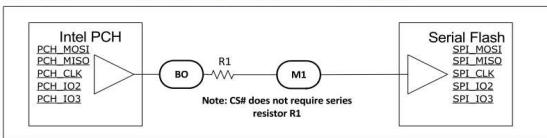


Figure 25-3. SPI Single Flash Device Routing Guidelines for CS#

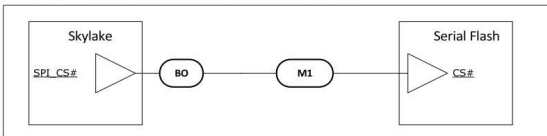
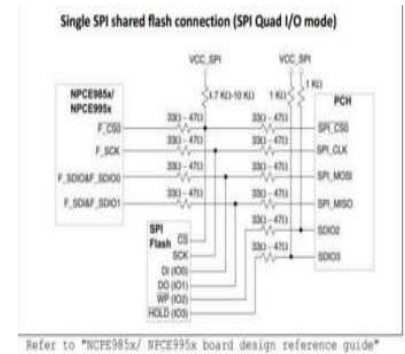


Table 22-3. SPI Single Flash Device Routing Guidelines (Sheet 2 of 2)

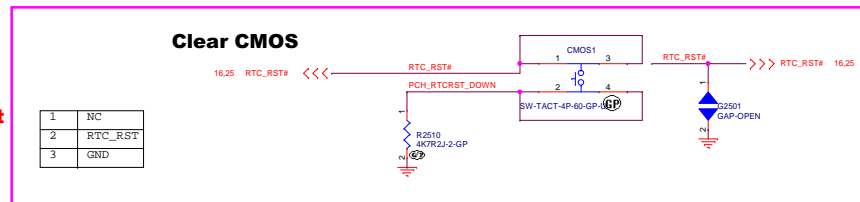
Parameter	Segment	Stackup	Unit	Routing Recommendation
Breakout Trace Length	BO	MS,SL	inch	<1"
Length 1	M1	MS,SL	inch	1"-5"
Length 2	M2	MS,SL	inch	0.5"-1"
Total length	BO, M1, M2	MS,SL	inch	1.5" - 7"
Resistor	R1		ohm	15
Resistor	R2		ohm	1k



**SSID = RBATT**

-1 for RTC Leakage

**2011/9/30**  
**Add CLR CMOS circuit**



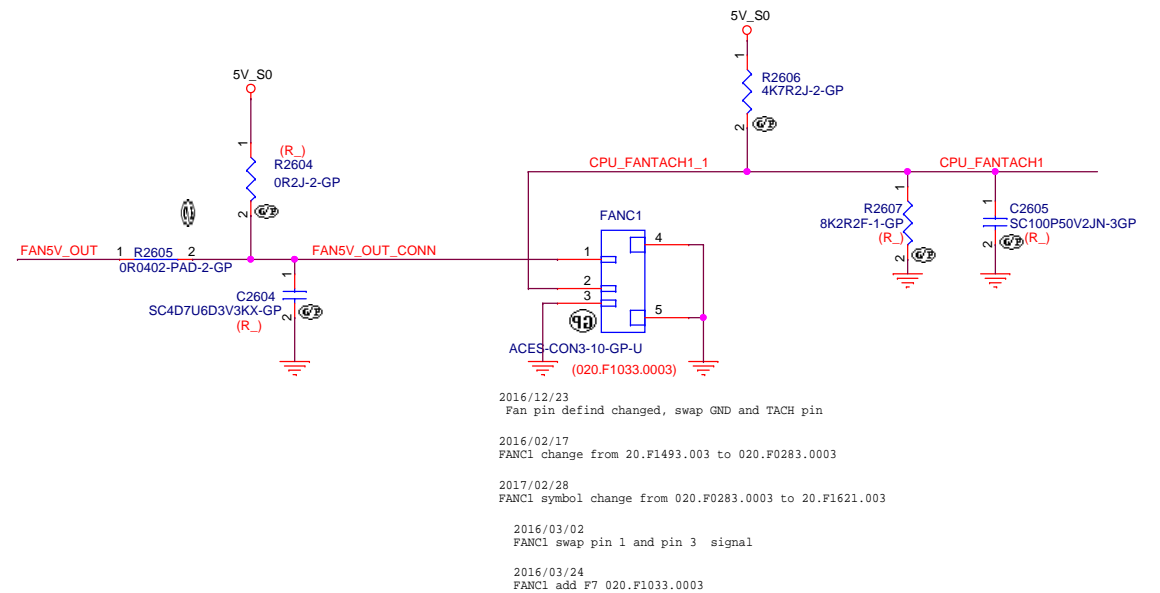
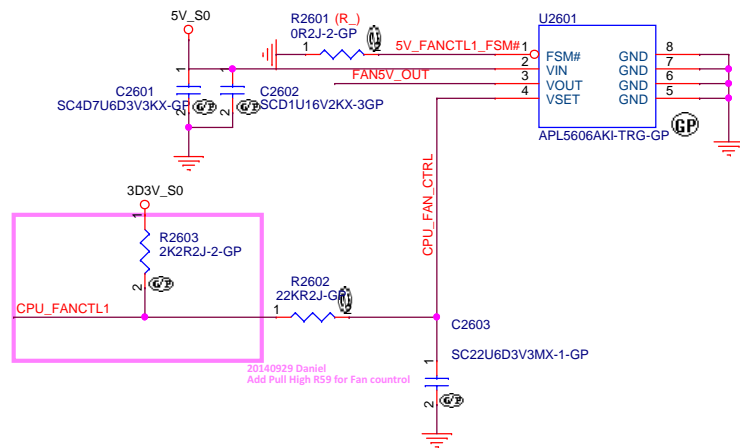
<Core Design>

**緯創資通** **Wistron Corporation**  
21F, 8F, Sec. 1, Hsin 1st Yih Rd., Hsinchu,  
Taipéi Hsien 221, Taiwan, R.O.C.

File **SPI/RTC**  
Size **Document Number**  
A2 **Eiffel215-KBL\_U** Rev **-1**  
Date: Saturday, May 06, 2017 Sheet 25 of 106



### FAN CTRL 5V



2016/12/23  
Fan pin defind changed, swap GND and TACH pin

2016/02/17  
FANCL change from 20.F1493.003 to 020.F0283.0003

2017/02/28  
FANCL symbol change from 020.F0283.0003 to 20.F1621.003

2016/03/02  
FANCL swap pin 1 and pin 3 signal

2016/03/24  
FANCL add F7 020.F1033.0003

<Core Design>

緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**FAN**

Size

Document Number

Custom

Eiffel215i-KBL U

Date:

Saturday, May 06, 2017

Sheet

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of

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Rev

-1

18	HDA_SDIN0_CPU	←
18	HDA_SDOUT_CODEC	→
18	HDA_SYNC_CODEC	→
18	HDA_BITCLK_CODEC	→
18,27	HDA_RST#_CODEC	→

```

90  DMIC_SDA_CODEC  >>>
90  DMIC_SCL_CODEC  >>>

```

18 HDA\_SPKR >>> \_\_\_\_\_

29 AUD\_SPK\_L+ <<<>>> \_\_\_\_\_

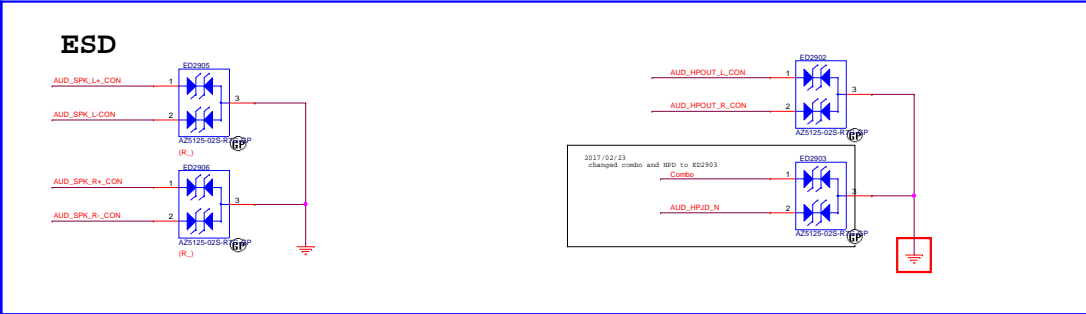
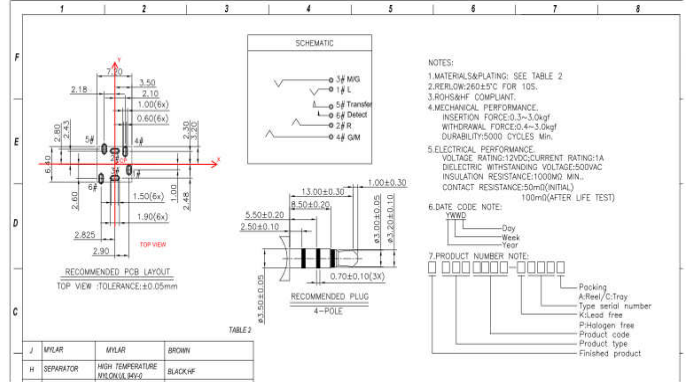
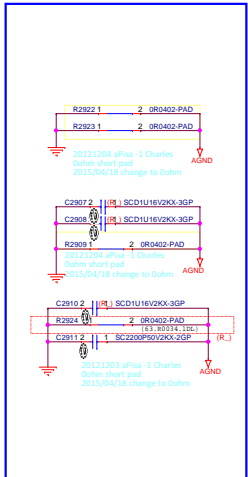
29 AUD\_SPK\_L- <<<>>> \_\_\_\_\_

29 AUD\_SPK\_R- <<<>>> \_\_\_\_\_

29 AUD\_SPK\_R+ <<<>>> \_\_\_\_\_

MAX: 0.866 A

MAX: 0.866 A





BLANK

<Variant Name>

		<b>Wistron Incorporated</b> 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title RSVD		
Size A	Document Number Eiffel215i-KBL_U	Rev -1
Date: Saturday, May 06, 2017		Sheet 30 of 105

15 LAN\_PCIE\_TX\_P  
15 LAN\_PCIE\_TX\_N  
15 LAN\_PCIE\_RX\_N  
15 LAN\_PCIE\_RX\_P

```

16 LAN_CLK_CPU      >>>
16 LAN_CLK_CPU_N    >>>
16 LAN_CLKREQ_CPU_N <<<

```

```

32 LAN_LINK_N
32 LAN_SPEED_100_N
32 LAN_SPEED_1000_N

```

32 LAN\_MDIO\_DP  
32 LAN\_MDIO\_DN

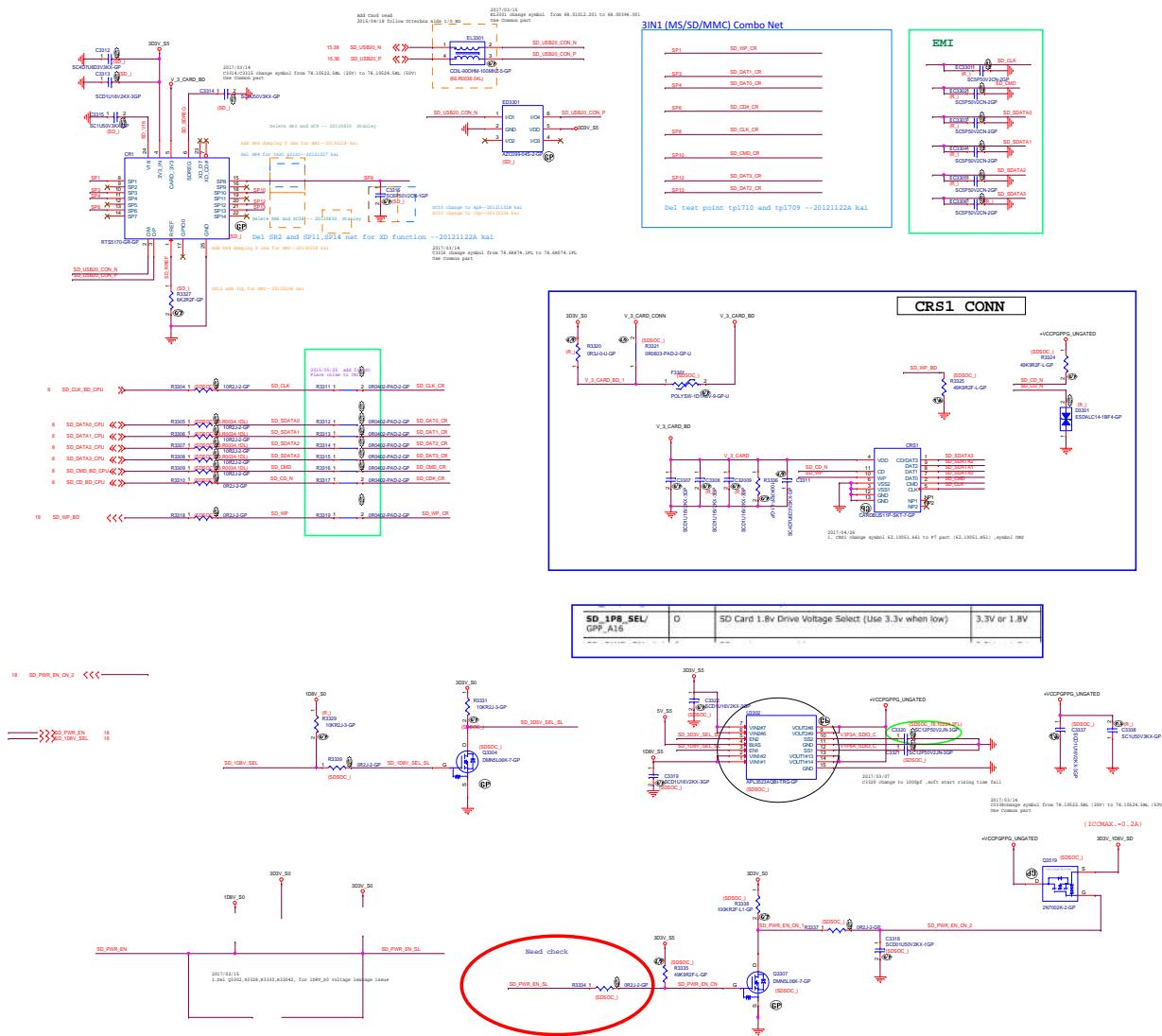
32 LAN\_MD1\_DP  
32 LAN\_MD1\_DN

32 LAN\_MD2\_DP  
32 LAN\_MD2\_DN

32 LAN\_MD3\_DP  
32 LAN\_MD3\_DN

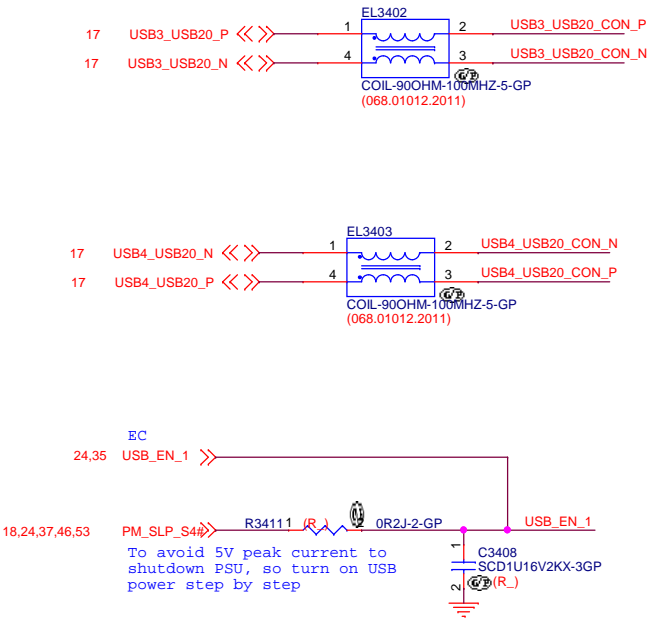




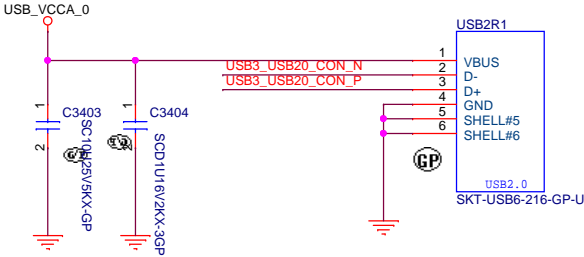
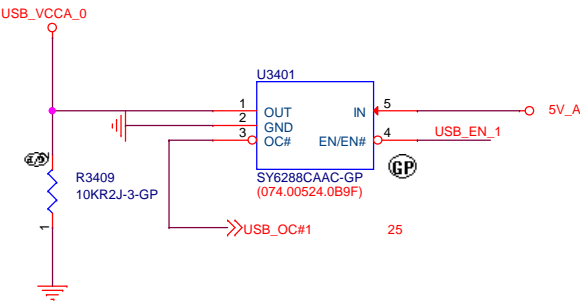
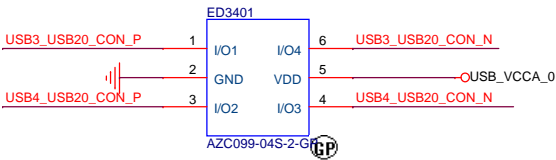
SSID = SDIO *Card Reader*

USB Port 3,4 -> Rear CONN

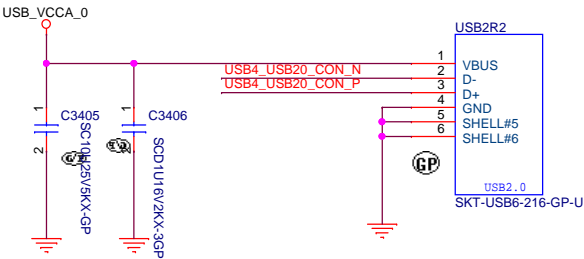
2017/03/14  
C3403/C3405 change symbol from 78.10623.51L(10V) to 78.10622.51L(25V)  
Use Common part



2017/03/14  
C3408 change symbol from 78.10491.4FL(Y5V) to 78.10421.2FL (X5R)  
Use Common part



2017/02/16  
1. USB2R1/USB2R2 change from 022.10005.01E1 to 022.10005.07D1



<Core Design>

<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>USB2/TOUCH CONN</b>		
Size Custom	Document Number <b>Eiffel215i-KBL U</b>	Rev <b>-1</b>
Date: Saturday, May 06, 2017	Sheet 34 of 105	

# Rear USB3.0

15.35 USB1\_USB30\_TX\_N >>  
 15.35 USB1\_USB30\_TX\_P >>  
 15.35 USB1\_USB30\_RX\_N <<  
 15.35 USB1\_USB30\_RX\_P <<

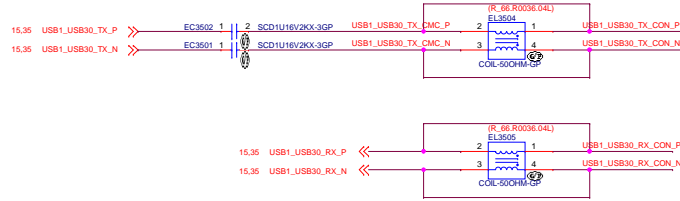
15.35 USB1\_USB20\_N <<  
 15.35 USB1\_USB20\_P <<

15.35 USB2\_USB30\_TX\_N >>  
 15.35 USB2\_USB30\_TX\_P >>  
 15.35 USB2\_USB30\_RX\_N >>  
 15.35 USB2\_USB30\_RX\_P >>

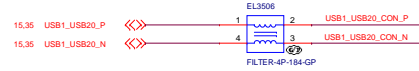
15.35 USB2\_USB20\_N >>  
 15.35 USB2\_USB20\_P >>

20.24,40.52 PM\_SLP\_S4# >>  
 24.34 USB\_EN\_1 >>  
 15.36 USB\_OC# <<

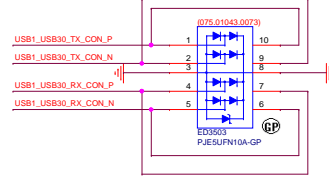
## USB3.0 EMI



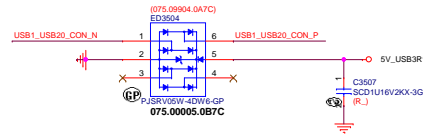
## USB2.0 EMI



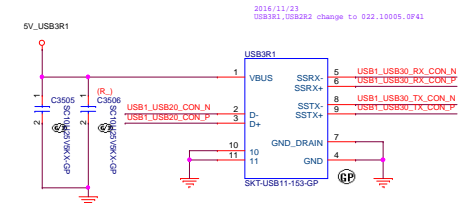
## USB3.0 ESD



## USB2.0 ESD

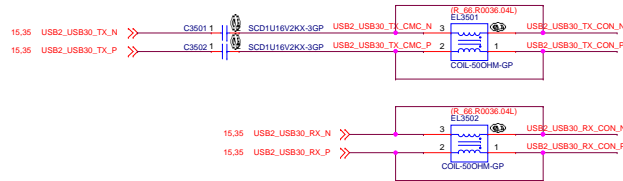


## USB3.0 Ext. port 1 (REAR)

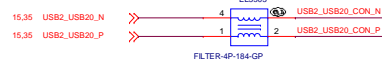


2017/03/14  
 C3505/C3503 /C3504/C3506 change symbol from 78.10623.51L(10V) to 78.10622.51L(20V)  
 Use Common part

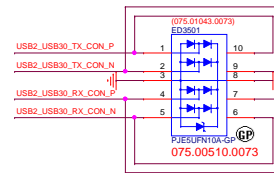
## USB3.0 EMI



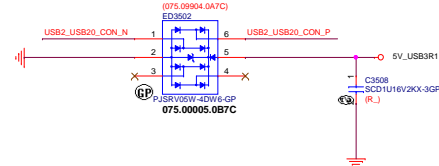
## USB2.0 EMI



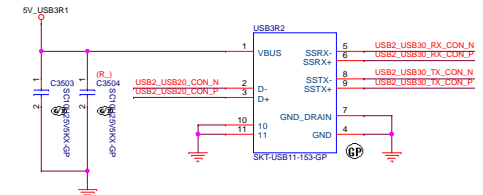
## USB3.0 ESD



## USB2.0 ESD

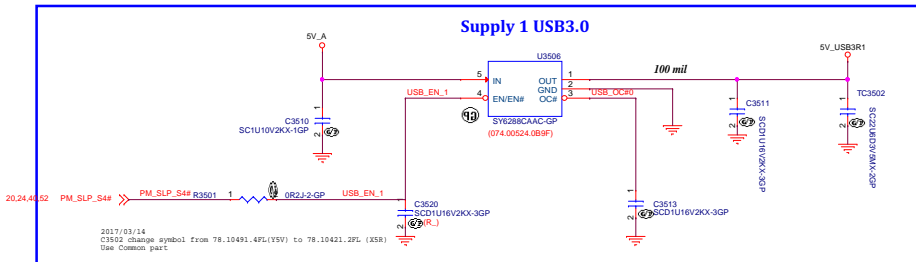


## USB3.0 Ext. port 2 (REAR)



## USB 3.0 Connector Pin definition

1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+ SuperSpeed RX
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+ SuperSpeed TX



2017/03/14  
 C3502 change symbol from 78.10491.4PL(15V) to 78.10421.2PL (XSR)  
 Use Common part

<Core Design>

緯創資通 Wistron Corporation  
 21F, 8F, Sec.1, Hsin Tai Wu Rd., Hsinchu,  
 Taipei Hsien 221, Taiwan, R.O.C.

File	USB3 CONN	Rev	-1
Sim	Document Number		
Customer	Eiffel215i-KBL U		
Date	Saturday, May 14, 2017	Printed	105

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<Core Design>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (RSVD)			
Size A4	Document Number Eiffel215i-KBL U		Rev -1
Date: Saturday, May 06, 2017		Sheet 36 of	105



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<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>(RSVD)</b>			
Size A	Document Number <b>Eiffel215i-KBL U</b>		Rev <b>-1</b>
Date: Saturday, May 06, 2017		Sheet 37 of	105

## Sheet 38 of 105

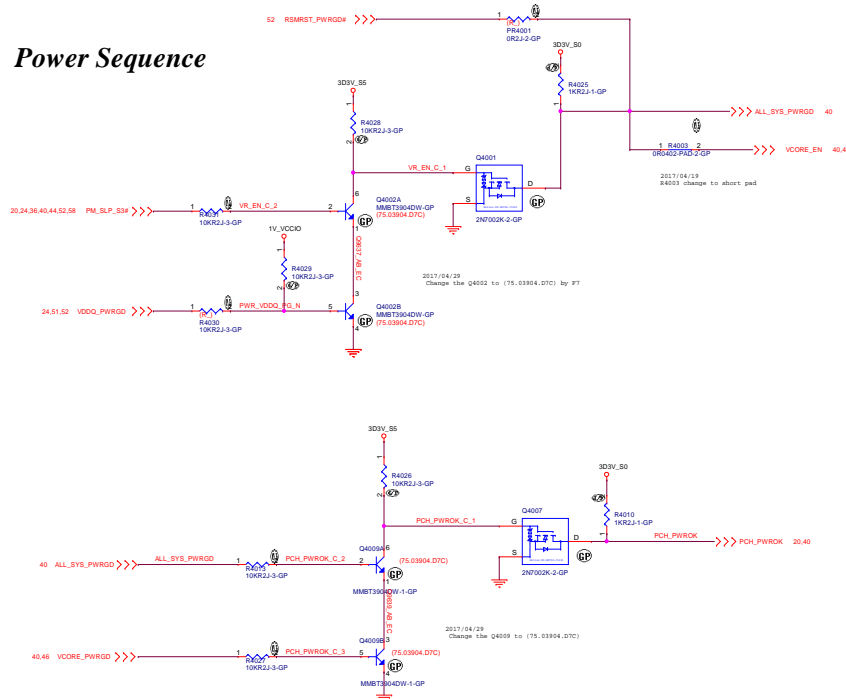
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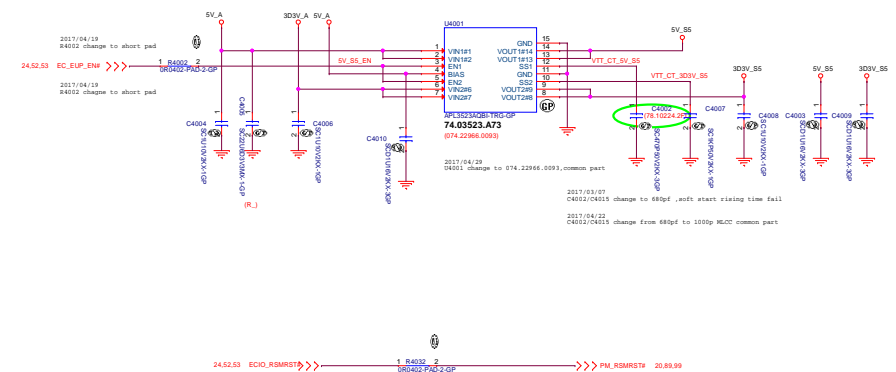
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>RSVD</b>			
Size A	Document Number <b>Eiffel215i-KBL U</b>		Rev <b>-1</b>
Date: Saturday, May 06, 2017		Sheet 39	of 105

## System

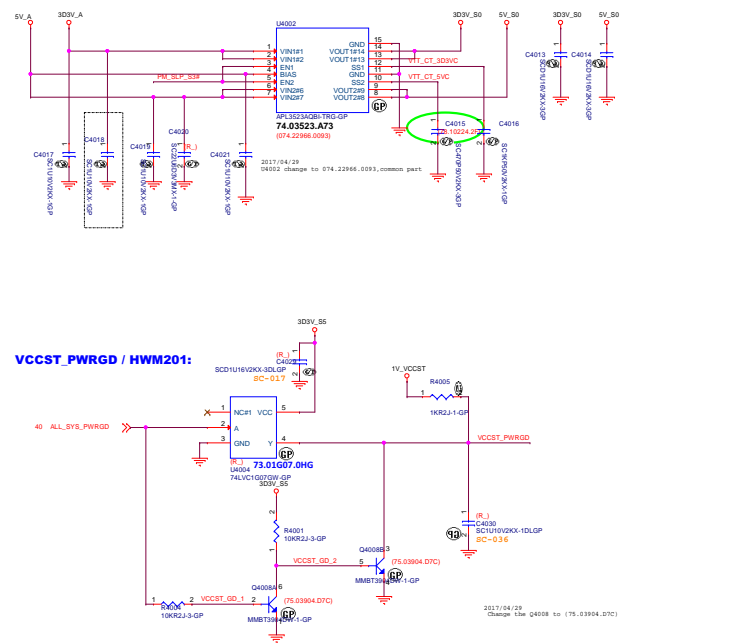
### *Power Sequence*



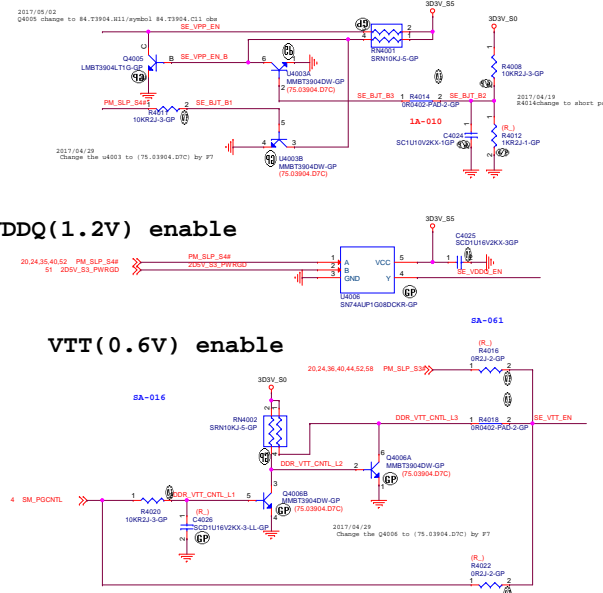
## 3D3V\_S5&5V\_S5



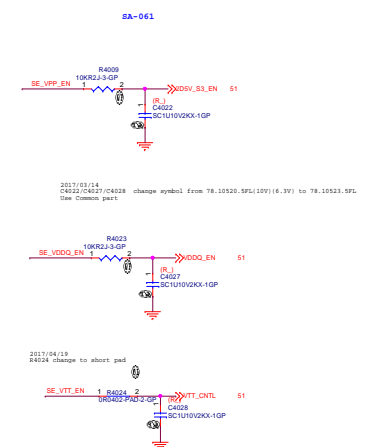
## 3D3V\_S0&5V\_S0



## DDR4 Power Sequence



```
VPP(2.5V) enable
```



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<Core Design>

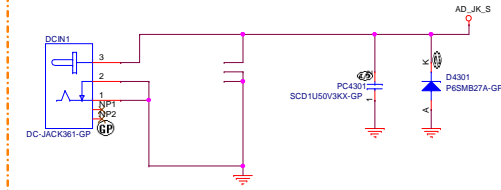
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>RSVD</b>			
Size A	Document Number <b>Eiffel215i-KBL U</b>		Rev <b>-1</b>
Date: Saturday, May 06, 2017		Sheet 41 of	105

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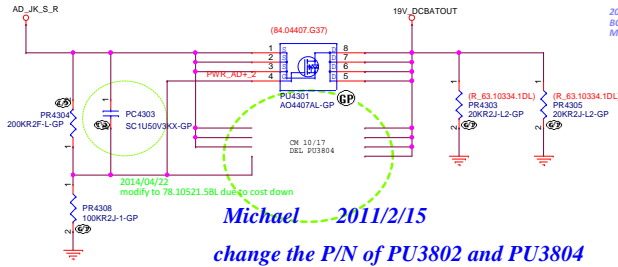
<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>RSVD</b>			
Size A	Document Number <b>Eiffel215i-KBL U</b>		Rev <b>-1</b>
Date: Saturday, May 06, 2017		Sheet 42 of	105

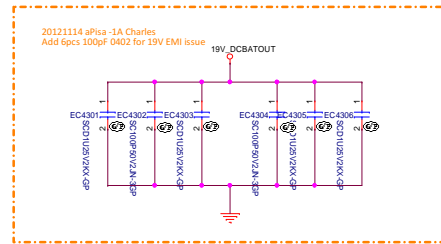
## ANNIE solution



20141216 DCIN1 PN Change to 022.10015.0371



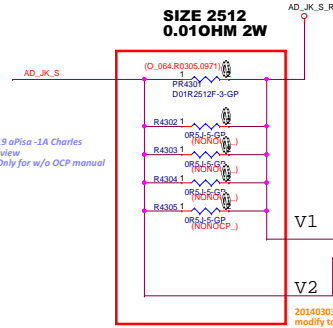
Michael 2011/2/15  
change the P/N of PU3802 and PU3804



20121114 aPisa -1A Charles  
Add 6pcs 100pF 0402 for 19V EMI issue

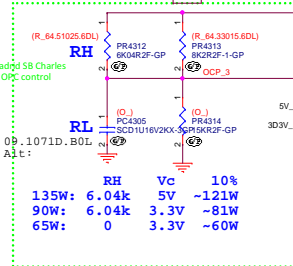
20121119 aPisa -1A Charles  
BOM Review  
Mount Only for w/o OCP manual

SIZE 2512  
0.010OHM 2W



20140303 Madrid-1 Charles  
modify to 30Kohm

20131127 Madrid SB Charles  
follow seatll OCP control

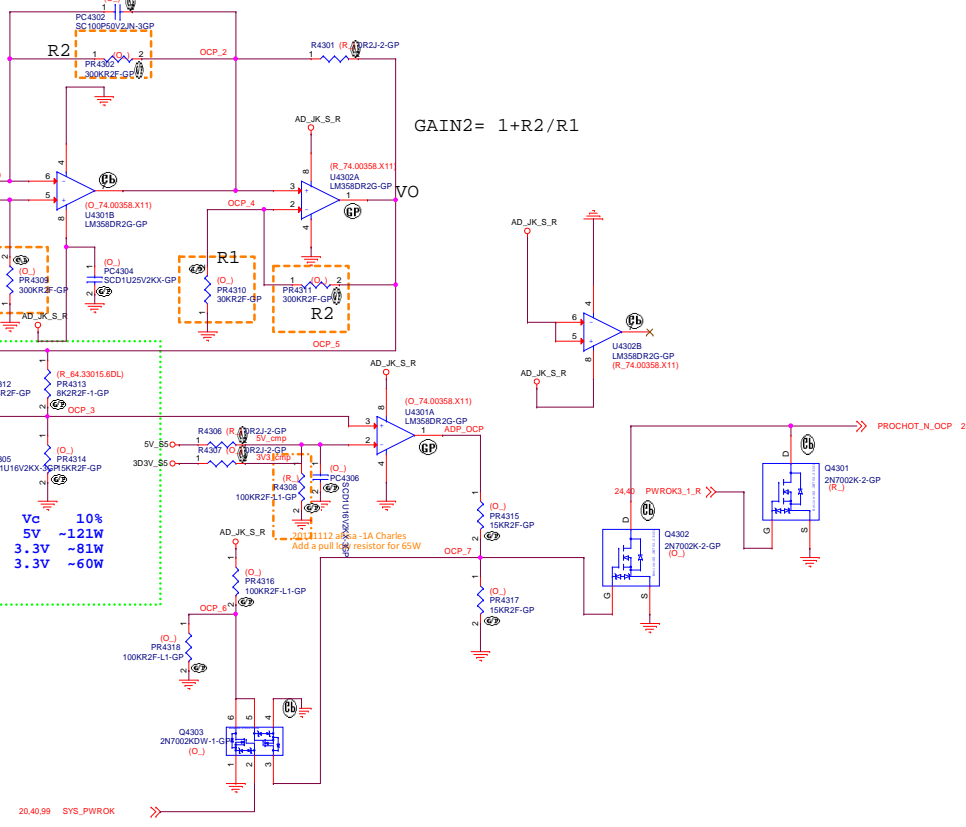


0.1071D.B0L  
A1 t:

RH Vc 10%  
135W: 6.04k 5V -121W  
90W: 6.04k 3.3V -81W  
65W: 0 3.3V -60W

$$GAIN1 = VO / (V2 - V1) = R2 / R1$$

$$GAIN2 = 1 + R2 / R1$$



<Core Design>

緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.

Title DC IN CONN

Size A2 Document Number Eiffe1215-KBL\_U Rev -1

Date: Saturday, May 04, 2013 Pages: 3 of 100

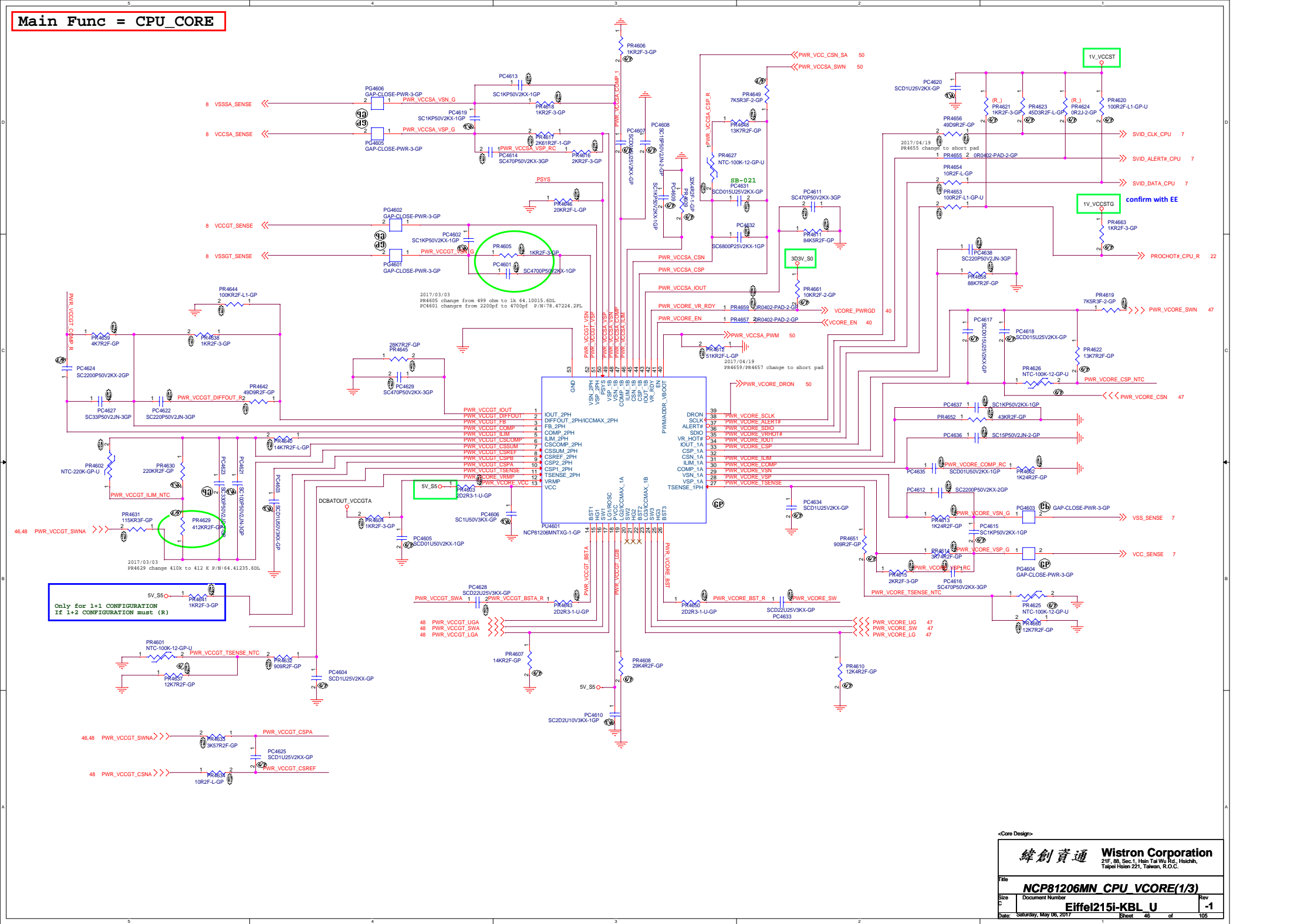
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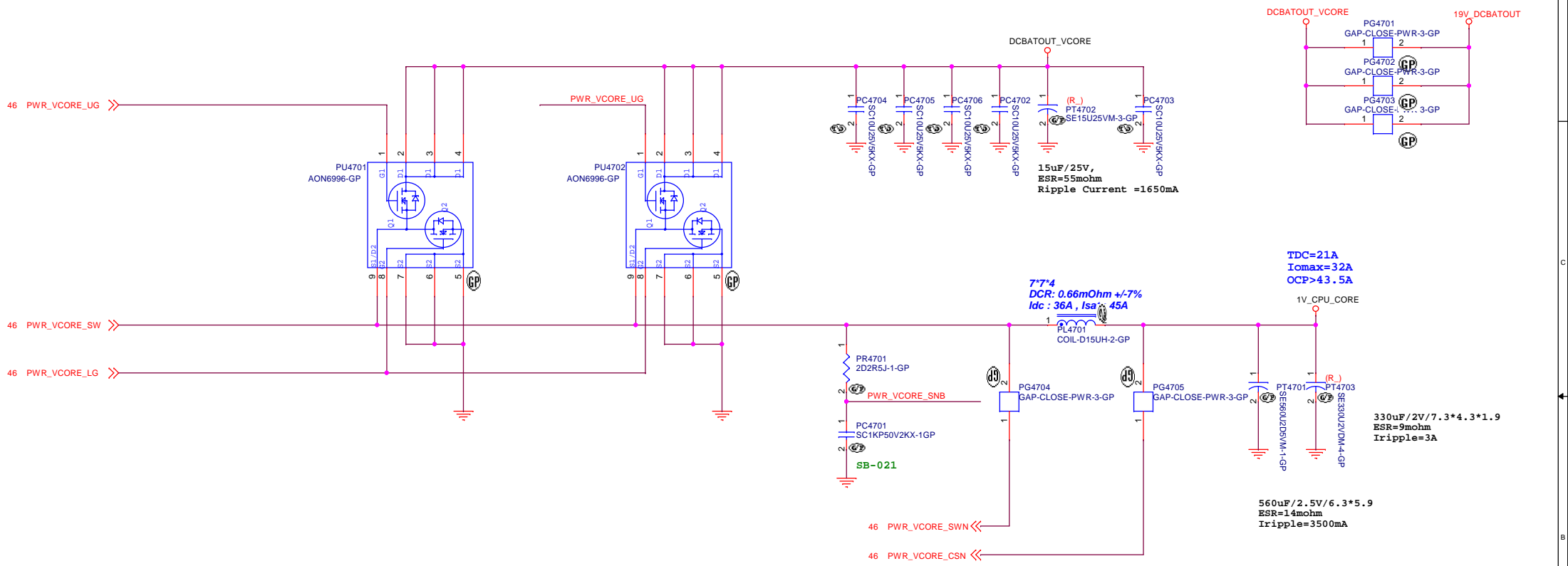
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Eiffel215i-KBL_U		
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
RSVD		
Size A4	Document Number	Rev -1
Date: Saturday, May 06, 2017		Sheet 44 of 105

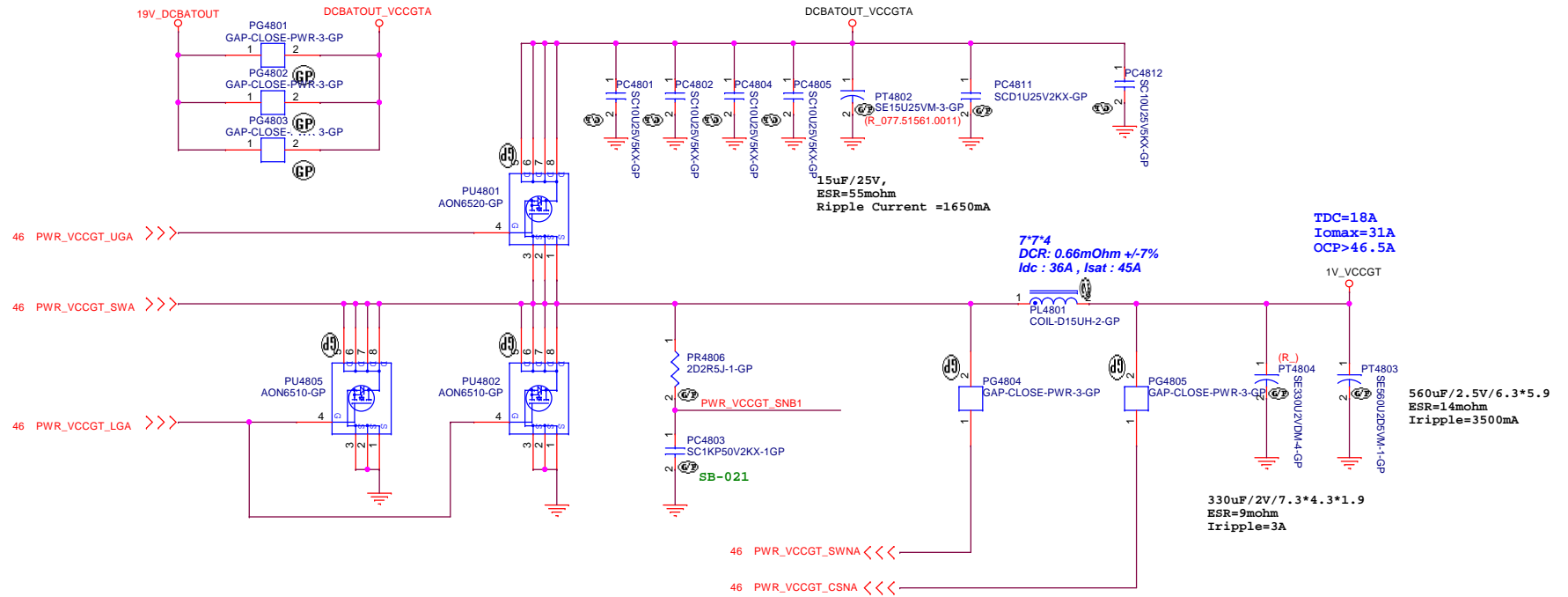




```
Main Func = CPU_CORE
```







<Core Design>

<b>緯創資通</b>		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>NCP81206MN CPU VCCGT(3/3)</b>			
Size A3	Document Number		Rev <b>-1</b>
Date:	<b>Saturday, May 06, 2017</b>	Sheet <b>48</b>	of <b>106</b>

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<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>IR Power</b>		
Size A	Document Number <b>Eiffel215i-KBL U</b>	Rev <b>-1</b>
Date: Saturday, May 06, 2017		Sheet 49 of 105



SSID = PWR.Plane.Regulator\_1p2v0p6v

VDDQ POWER GOOD

7.24.52 VDDQ\_PWRGD

VDDQ ENABLE CONTROL

40 VDDQ\_EN

2017/04/19  
PR5127 change to short pad

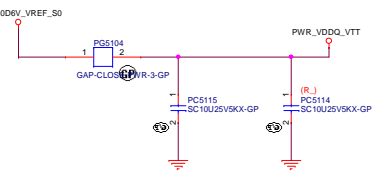
Freq. setting  
750K -> 350K Hz

Need EE confirm

0.51 VDDQ\_EN  
SC-027  
SC-037  
2017/04/19  
PR5113/PR5114 change to short pad

40 VTT\_CTL  
SC-027  
SC-037

Vout = 0.6V  
Iomax = 0.75A



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

OCP setting

VID  
Logic-High = 0.75V  
Logic-Low = 0.3V

84.04C10.037 NTMFS4C10N  
Rds(on) = 5.8-6.95 mohm,  
Vgs=10V, I-D = 30A,  
Qg = 18.9nC  
Vgs=10V, Vds=15V, I-D=30A

84.04C06.037 NTMFS4C06N  
Rds(on) = 3.2-4.0 mohm,  
Vgs=10V, I-D = 30A,  
Qg = 23nC  
Vgs=10V, Vds=15V, I-D=30A

VIN RIPPLE CURRENT Imax=2.32A

Idesign=9.5A  
14.25A<OCP<19A

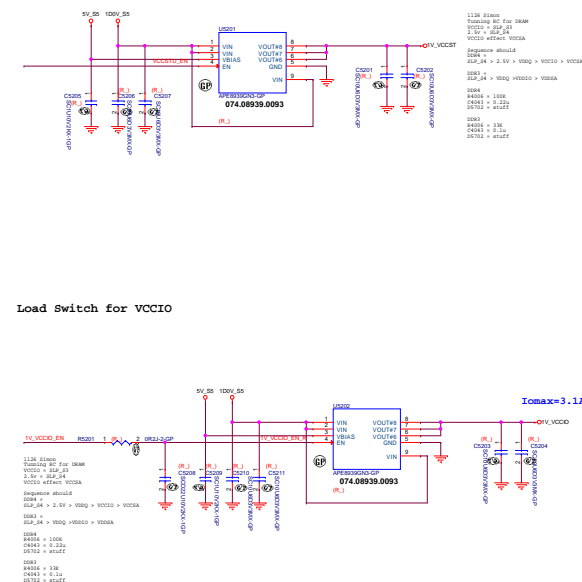
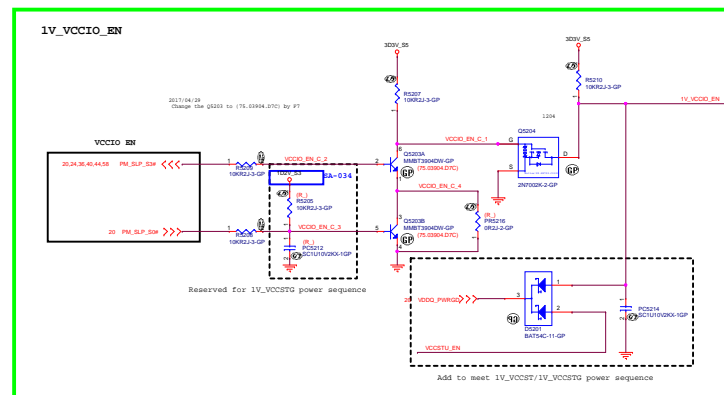
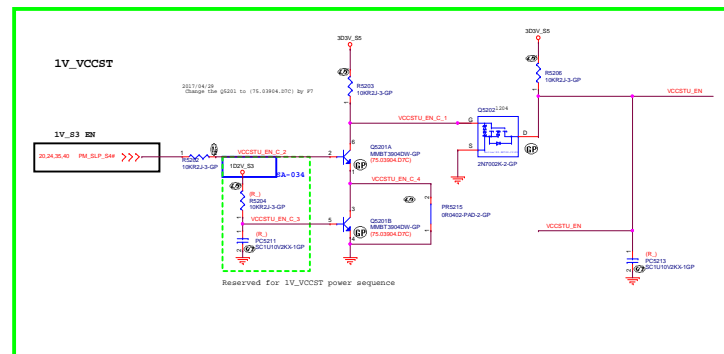
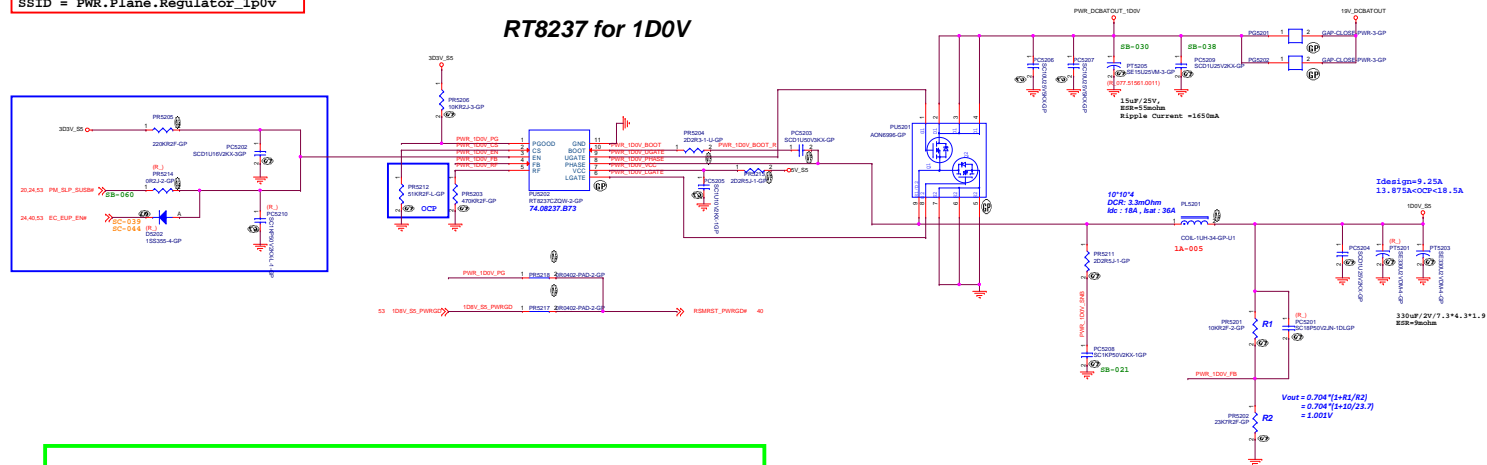
Vout Setting  
 $V_{out} = V_{ref} * (1 + R1/R2)$   
 $V_{out} = 0.675 * (1 + 15.8K / 20K)$   
 $V_{out} = 1.2V$

VID vs Vref Table  
VID Logic-High => Vref = 0.675 V  
VID Logic-Low => Vref = 0.75 V  
note: Vref can only be changed from  
0.675v to 0.75v after power-on

<Core Design>

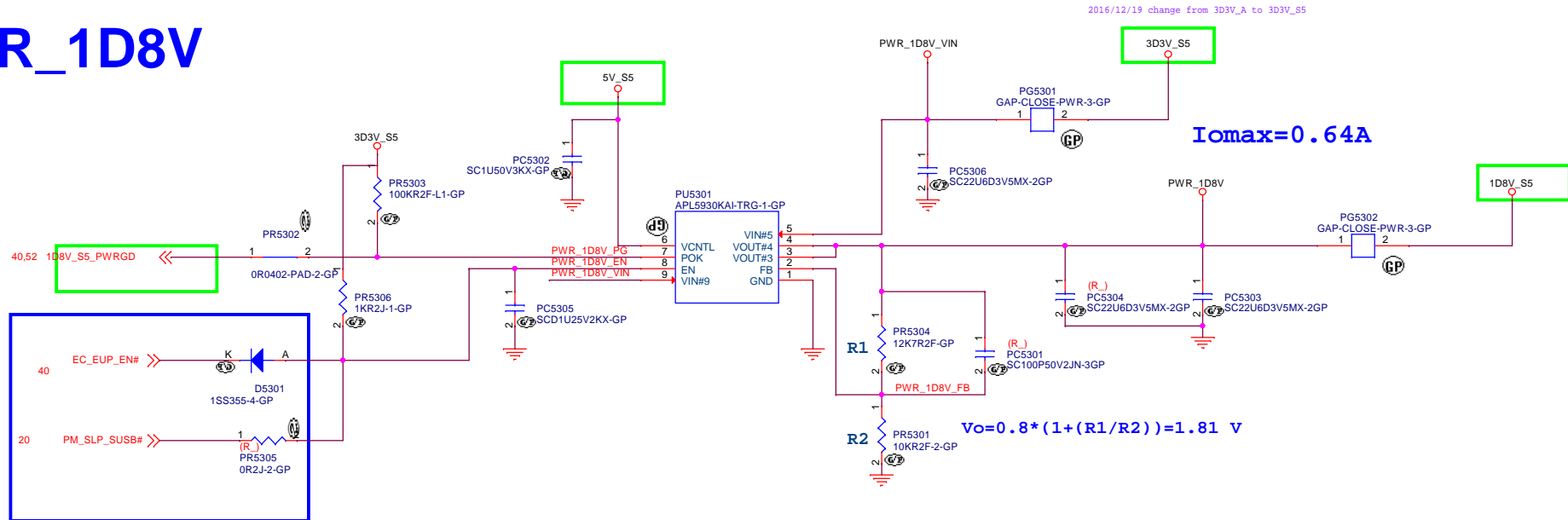
緯創資通 Wistron Corporation  
21F, 8F, Sec.1, Hsin Tai Wu Rd., Hsinshu,  
Taichung Hsien 221, Taiwan, R.O.C.

File	Document Number	Rev
VDDQ/VTT/2D5V S3	Eiffel215i-KBL U	-1
Size	Custom	
Date: Saturday, May 06, 2017	Sheet 51 of 106	

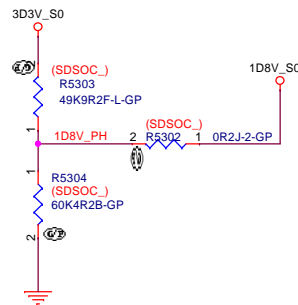
**RT8237 for 1D0V**[illegible]



# PWR\_1D8V



## 1D8V\_S5 to 1D8V\_S0



<Core Design>

<b>緯創資通</b>		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>G9661 1D8V S5</b>			
Size A3	Document Number		Rev <b>-1</b>
<b>Eiffel215i-KBL U</b>			
Date	Saturday, May 06, 2017	Sheet 53 of	105

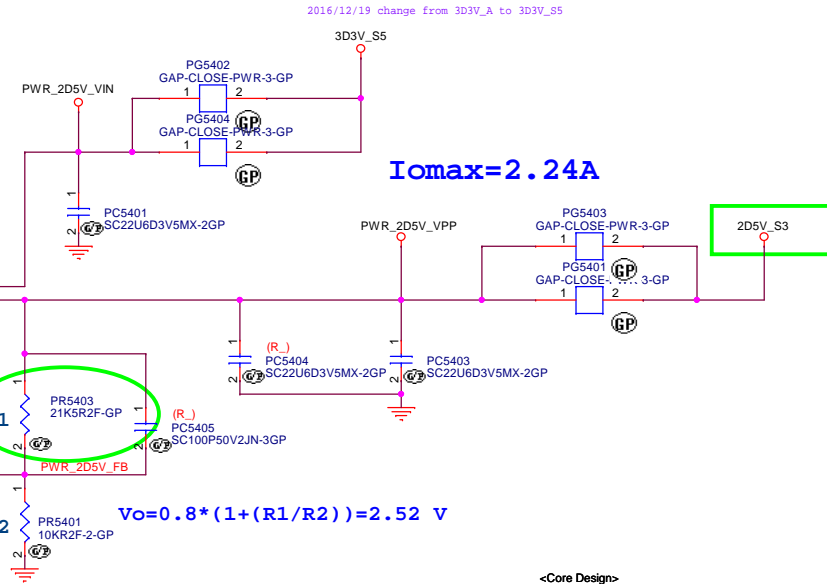
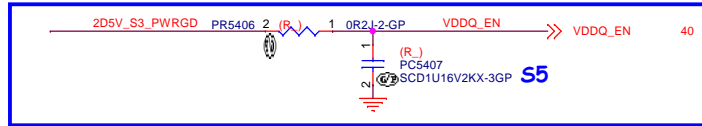
# PWR\_2D5V\_VPP

2D5V POWER Enable

40 2D5V\_S3\_EN

2D5V POWER GOOD

40 2D5V\_S3\_PWRGD



2017/02/24  
PR5403 changed from 21k to 21.5k

2016/12/19 change from 3D3V\_A to 3D3V\_S5

<Core Design>

緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**RSVD**

Size

Custom

Document Number

Date:

Saturday, May 06, 2017

Sheet

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of

105

**Eiffel215i-KBL U**

Rev

-1

```
SSID = VIDEO
```

LCD ID



CONVERTOR SMB



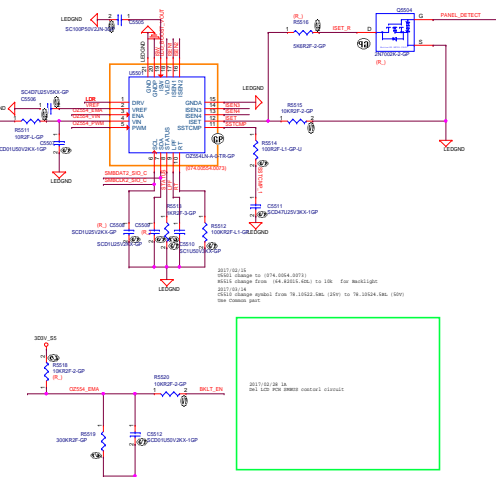
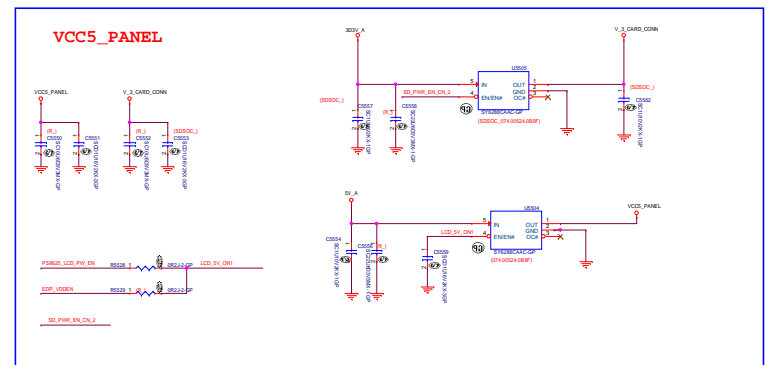
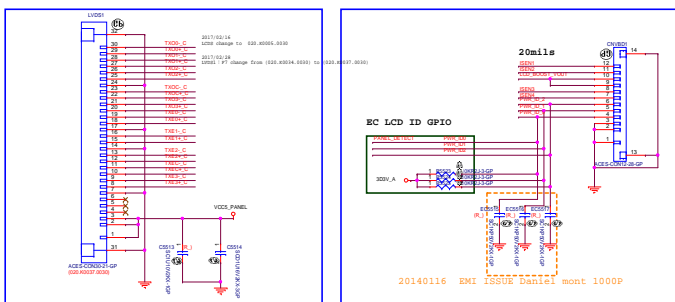
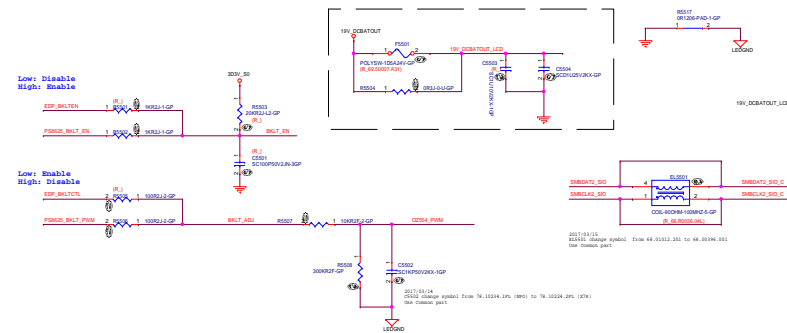
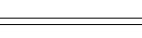
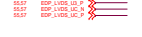
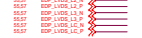
3 BOLT\_EN >>>



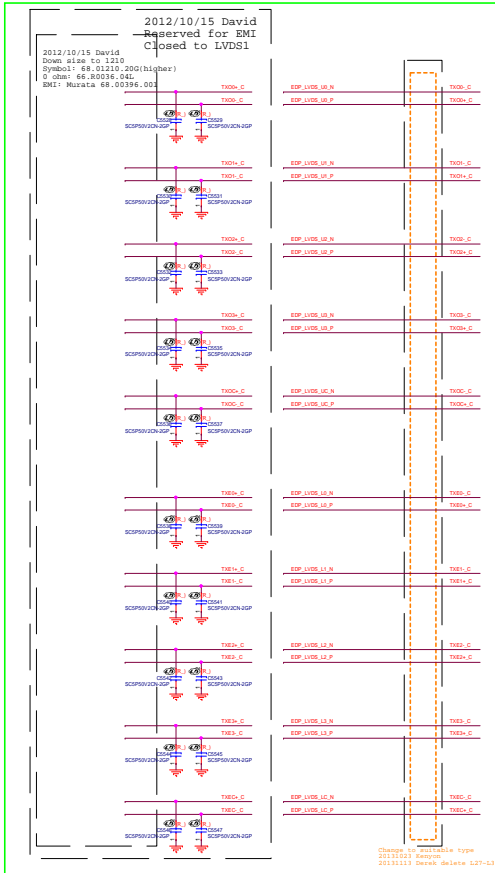
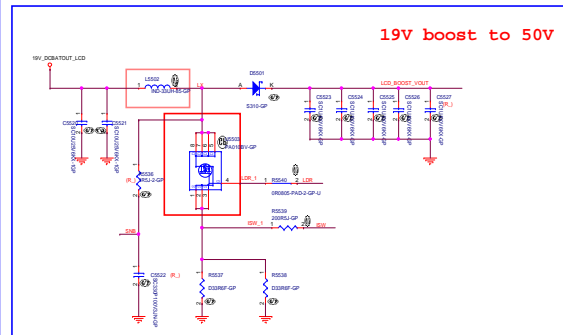
57 P58625\_LCD\_PW\_EN



## LVDS For eDP translator



Panel Model	Cable Spec			
	ID0	ID1	ID2	Vout
LG LM30W/F3-SLK1	0	0	0	3.4 Vout 1.6 RTN 2.5 N.C
LG LM30W/F5-TLF1	0	0	1	3.4 Vout 1.6 RTN 2.5 N.C
LG LM30W/F3-SLL1	0	1	0	3.4 Vout 1.6 RTN 2.5 N.C
CM1 M195FGE-423 C1	1	0	0	1.2,5.6 Vout 3.4 RTN
CM1 M195FGE-420 C3	1	1	0	1.2,5.6 Vout 3.4 RTN
CM1 M195FGE-420 C1	1	1	1	1.2,5.6 Vout 3.4 RTN



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<Core Design>

緯創資通

**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**RSVD**

Size  
A

Document Number

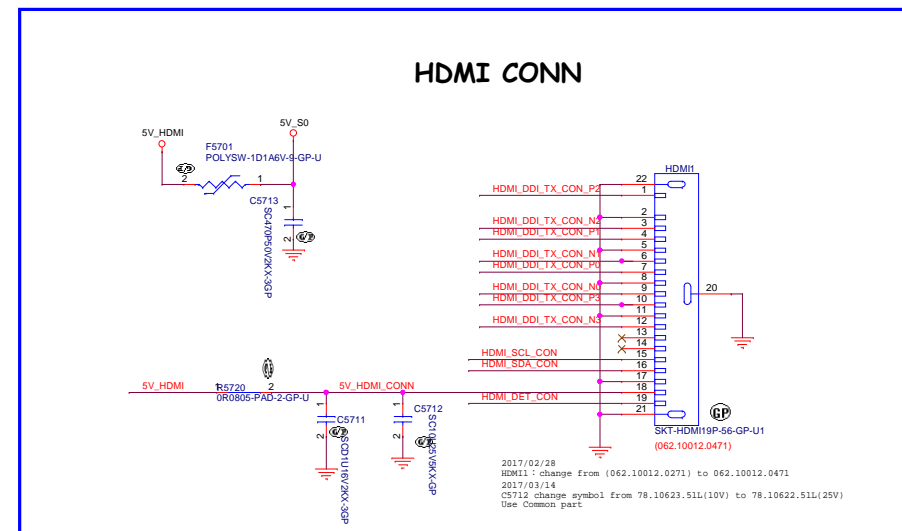
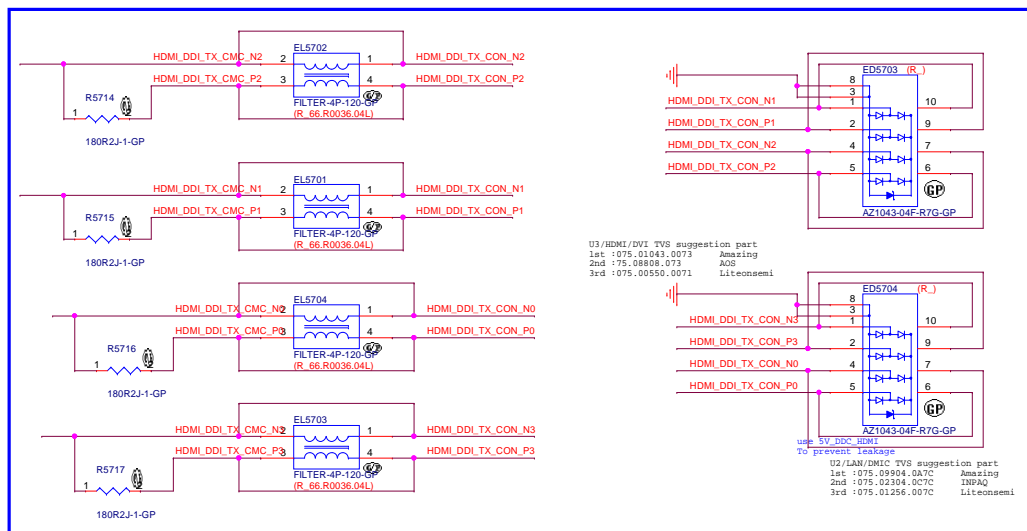
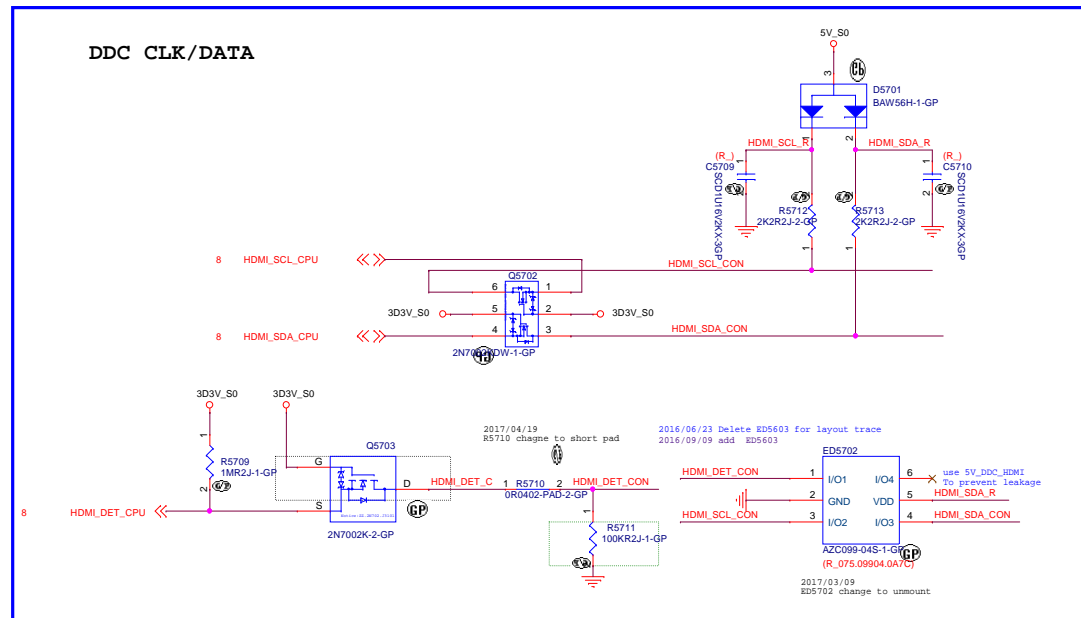
**Eiffel215i-KBL U**

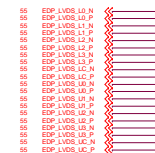
Rev

**-1**

Date: Saturday, May 06, 2017

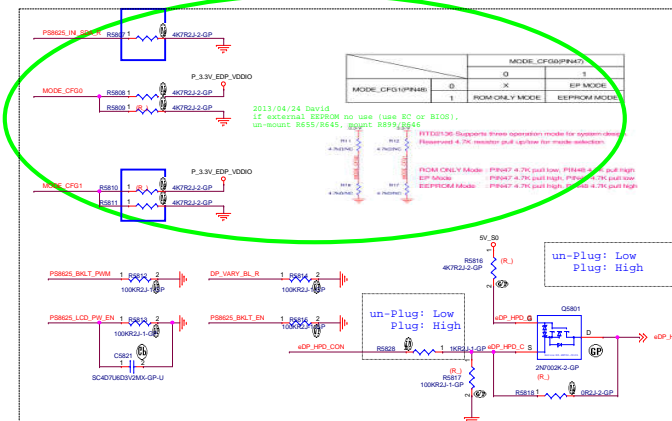
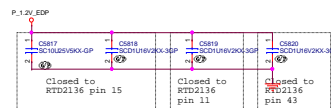
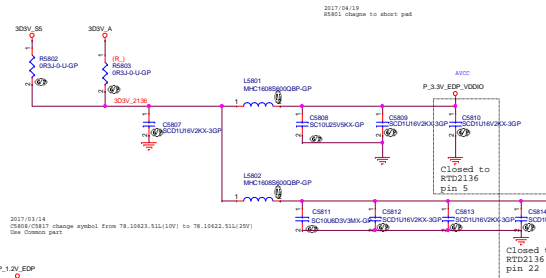
Sheet 56 of 105



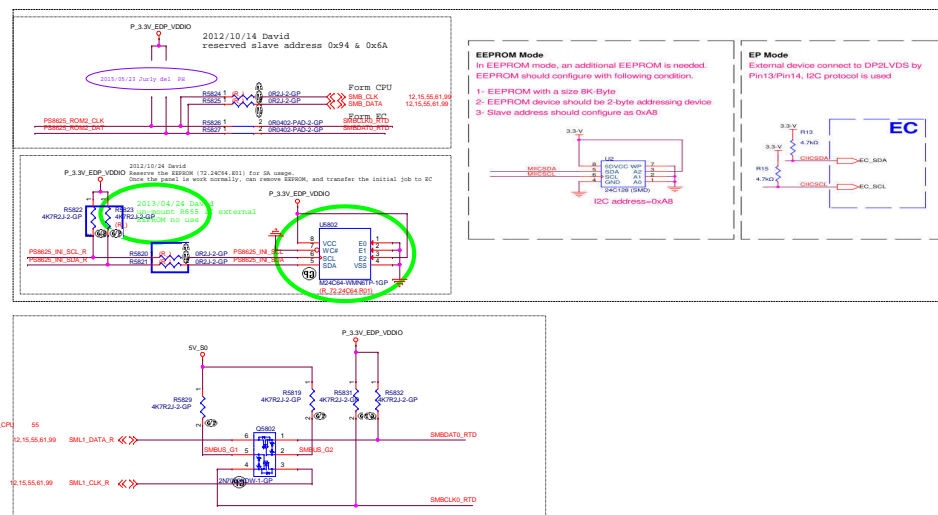
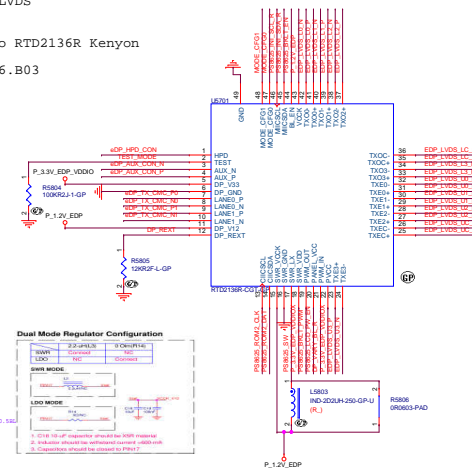


8.57 EDP\_HPD\_CPU <<>> EDP\_BKLCTL  
55 PS8625\_BKLT\_PWM <<>>  
55 PS8625\_LCD\_PW\_EN <<>>  
55 PS8625\_BKLT\_EN <<>>  
3.55 EDP\_BKLTCTL <<>> EDP\_BKLCTL

12,15,55,61,99	SML1_CLK_R	⌞⌞⌞⌞	=====
12,15,55,61,99	SML1_DATA_R	⌞⌞⌞⌞	=====
18,58,61	SMB_CLK	⌞⌞⌞⌞	=====
18,58,61	SMB_DATA	⌞⌞⌞⌞	=====



2012/11/07  
Change from PS8625 to RTD2136R Kenyon  
Copy from ROSA PBAIO  
RTK RTD2136R/71.02136.B03

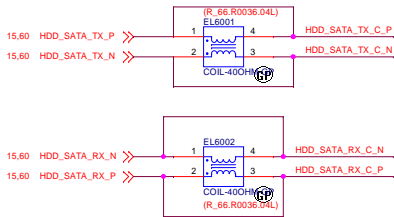


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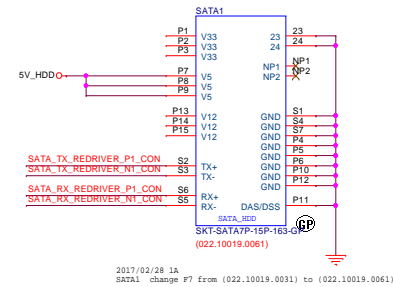
<Core Design>

<div>緯創資通</div>		<div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
Title			
RSVD			
Size A	Document Number		Rev
	Eiffel215i-KBL_U		-1
Date:	Saturday, May 06, 2017	Sheet 59 of	105

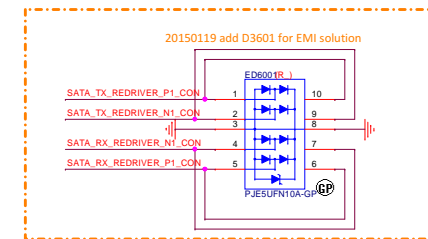
15.60 HDD\_SATA\_TX\_P  
15.60 HDD\_SATA\_TX\_N  
15.60 HDD\_SATA\_RX\_N  
15.60 HDD\_SATA\_RX\_P



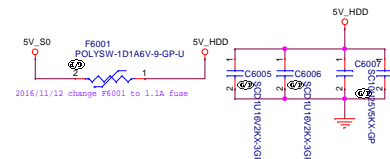
## SATA HDD Connector



2016/12/28  
del SATA Re-drvier circuit



Layout: Put them together

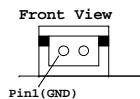


2017/03/14  
C6007/C6008 change symbol from 78.10623.51L(10V) to 78.10622.51L(25V)  
Use Common part

## SATA ODD/ Power Connector

20141202 Ruei oDD1 part number change to 020.80245.0007

ODD SATA POWER CONNECTOR



2012/08/18\_aPisa\_SA  
ADD ODD

20.60341.104: 4pin right angle  
20.60334.103: 3pin right angle

<Core Design>

緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu,  
Taipei Hsin 221, Taiwan, R.O.C.

File HDD/ODD

Size Document Number

Custom Effe215i-KBL\_U

Date: Saturday, May 06, 2017

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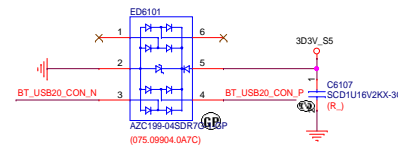
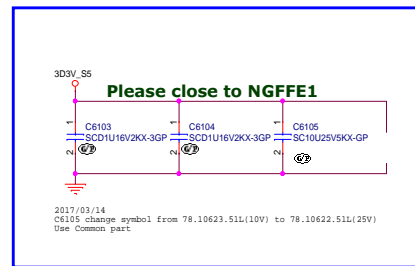
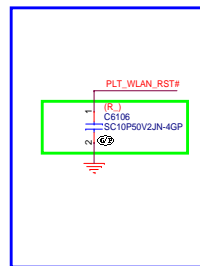
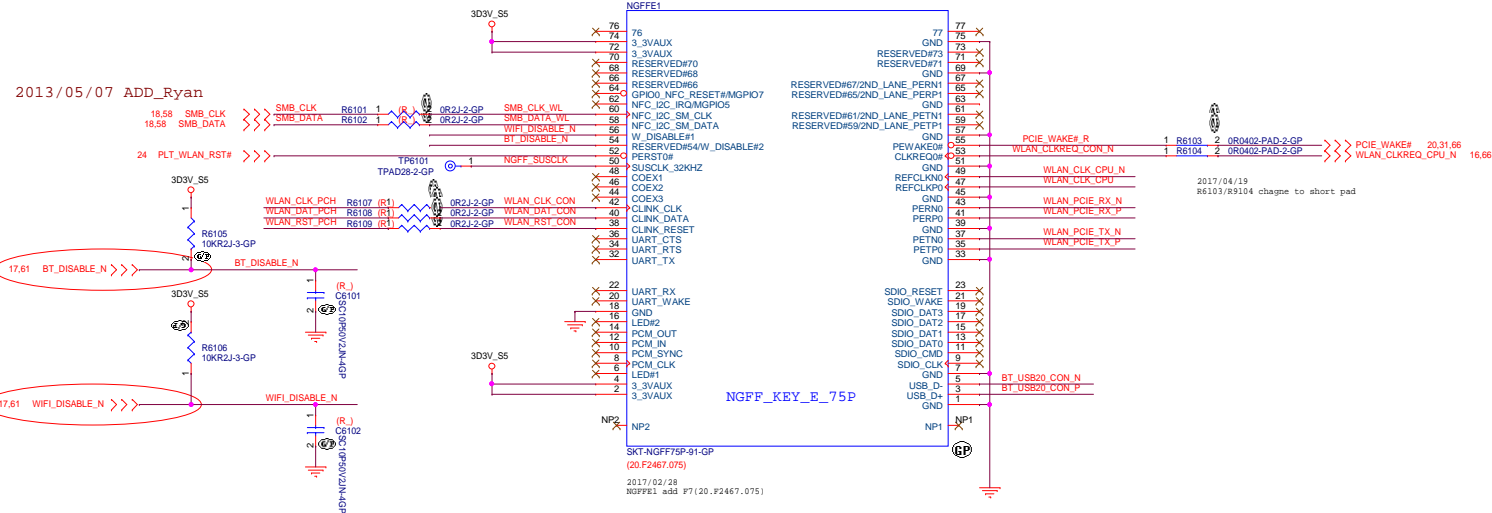
Rev -1



SSID = Wireless and Bluetooth

## M.2 2230 / 1630 Key E Type (Wireless LAN+BT)

### 20141218 MINI1 change to M.2



<Core Design>

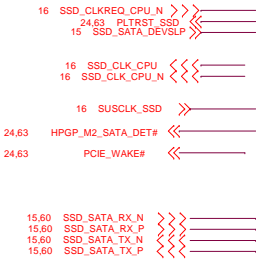
緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

File			Rev
WLAN CARD			-1
Size	Document Number	Eiffel215i-KBL_U	
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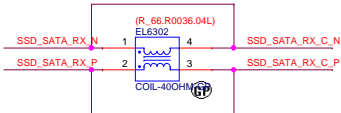
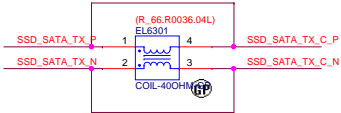
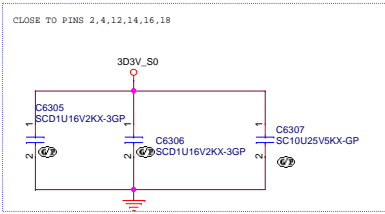
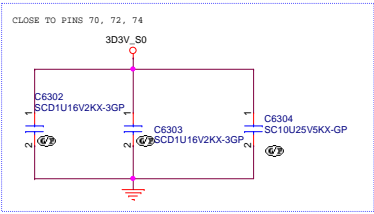
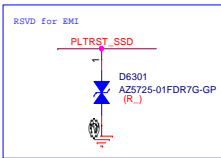
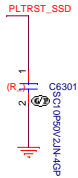
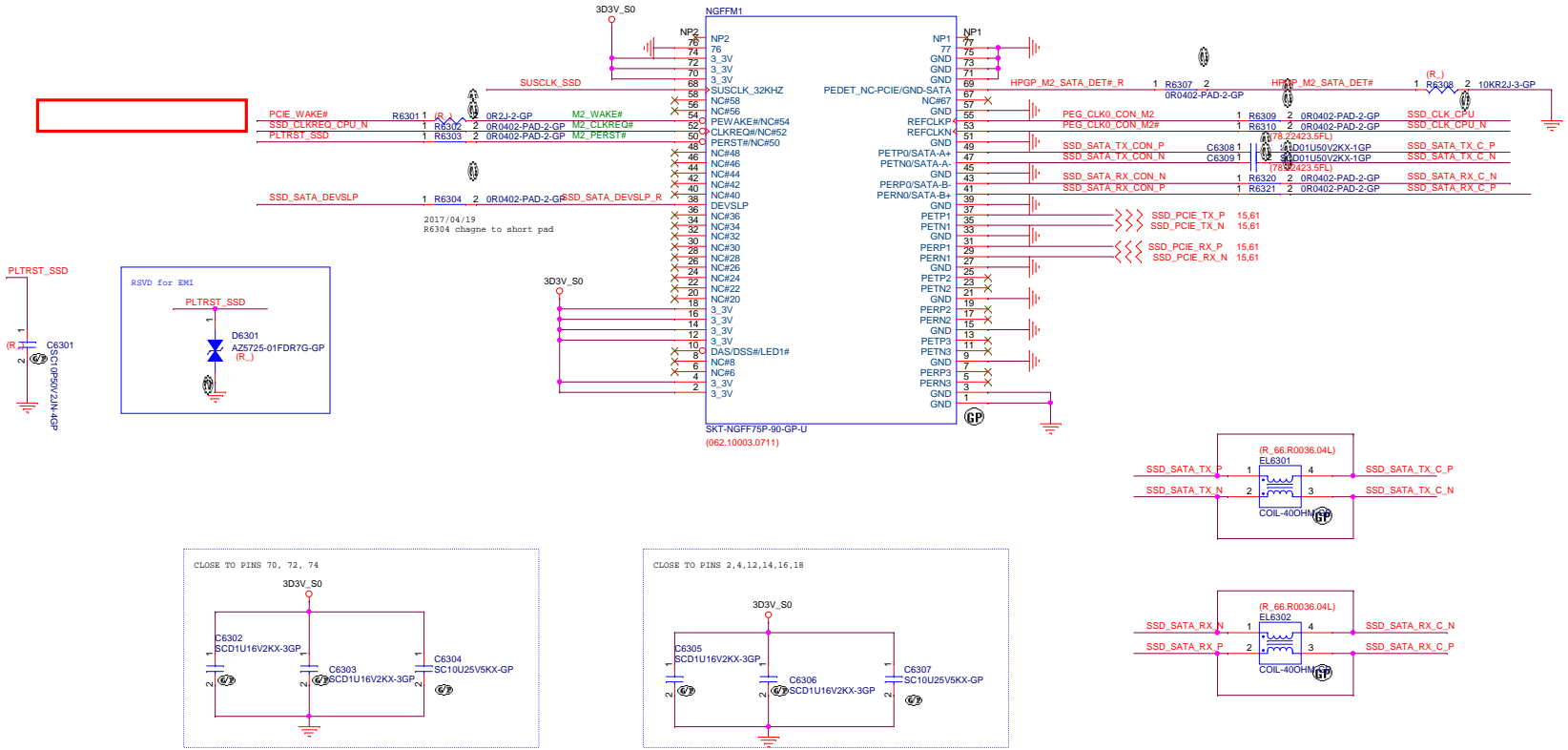
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Title <b>RSVD</b>			
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HPGP_M2_SATA_DET#	Module Type
0	SSD-SATA
1	SSD-PCIE

# M.2 Key M Type

2017/02/28  
NGFPM1 change to NGFPM1and add F7 062.10003.0711



2017/03/14  
C6304/C6307 change symbol from 78.10623.51L(10V) to 78.10622.51L(25V)  
Use Common part

<Core Design>

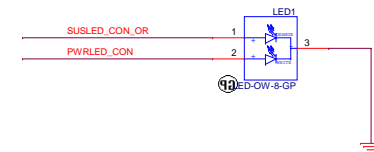
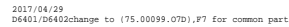
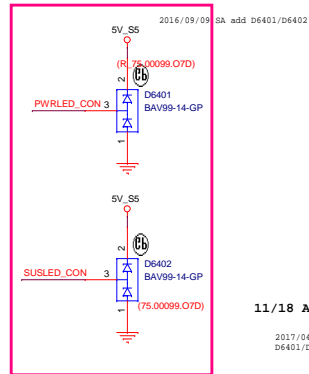
緯創資通

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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

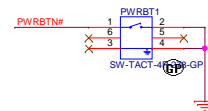
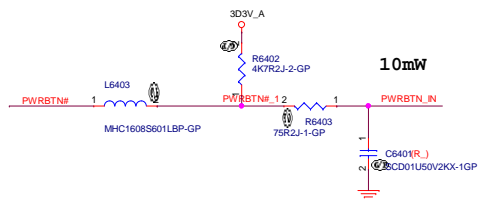
SSD

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24 SUSLED\_N >>



## 61 PWRBTN\_IN &lt;&lt;-----



2017/02/16  
PWRBT1 change from 022.40001.0661 to 062.40001.0141

2017/04/22  
PWRBT1 change from 062.40001.0142 to 062.40001.0851 by F7

```
2017/04/26
FWRBT1 symbol change from 062.40001.0142 to 062.40001.0B51
```

### <Core Design>

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title	<b>PWR BTN/SIDE KEY/LED</b>
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Size A	Document Number <b>Eiffel215i-KBL U</b>		Rev <b>-1</b>
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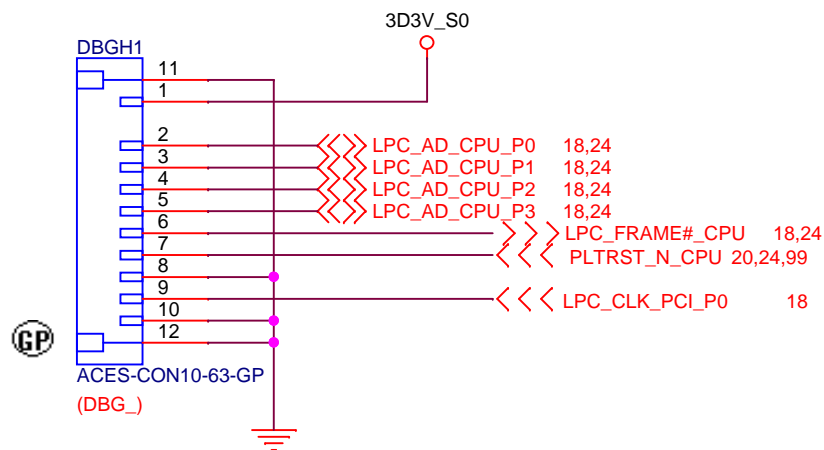
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2017/02/16  
change DBGH1 to 020.F0522.0010 Debug header interference. With SSD connector.

<Core Design>

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Title <div>DEBUG HEADER</div>	
Size A	<div>Document Number</div> <div>Eiffel215i-KBL_U</div>
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Size	Document Number	Rev
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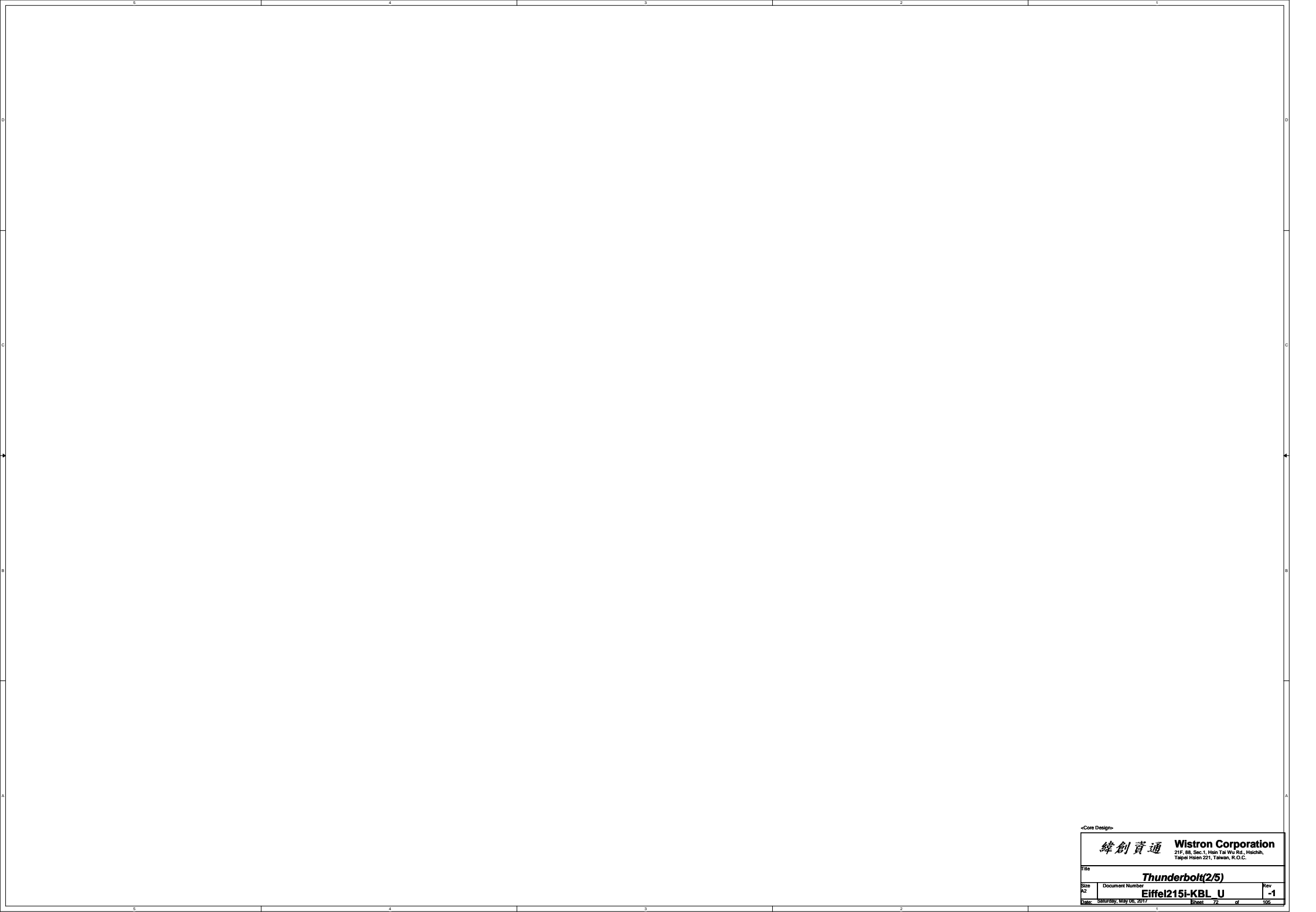
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C				C
B				B
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Title <div>Thunderbolt(1/5)</div>			
Size A	Document Number <div>Eiffel215i-KBL U</div>		Rev -1
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Thunderbolt(2/5)		
Size	Document Number	Rev
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Wistron Corporation

21F, 8B, Sec. 1, Hsin Tai Wu Rd., Hsichia, Taipei Hsien 221, Taiwan, R.O.C.

Title

Thunderbolt(3/5)

Size

Document Number

Rev

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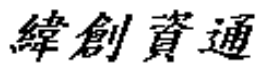
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Size A	Document Number <b>Eiffel215i-KBL_U</b>		Rev <b>-1</b>
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Title <b>GPU(2/5)_DIGITALOUT</b>			
Size A	Document Number <b>Eiffel215i-KBL_U</b>		Rev <b>-1</b>
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GPU(3/5)_VRAM			
Size	Project Name		Rev
	OPP_17D3_SKU		
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Title <b>GPU(4/5)_GPIO/STRAP</b>			
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Title <b>GPU(5/5)_PWR/GND</b>			
Size A	Document Number <b>Eiffel215i-KBL_U</b>		Rev <b>-1</b>
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Title <div>VRAM2/4</div>			
Size A	Document Number <div>Eiffel215i-KBL_U</div>		Rev <div>-1</div>
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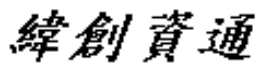
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Size A	Document Number <b>Eiffel215i-KBL_U</b>	Rev <b>-1</b>
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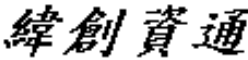
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Title <b>RSVD</b>			
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Title <b>RT8812 PWR VGA CORE</b>			
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Title <b>+V 3P3 VGA/1D35V VGA/+V 1P05 VGA</b>		
Size A	Document Number <b>Eiffel215i-KBL U</b>	Rev <b>-1</b>
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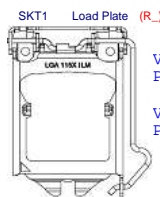
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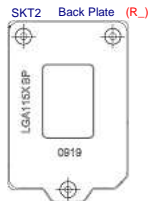
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Title <b>RSVD</b>		
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Material part

LGA115x CPU SOCKET Symbol



Vendor: LOTES  
P/N: 22.78003.011  
  
Vendor: FOXCONN  
P/N: 22.78006.001

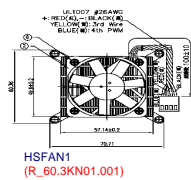


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P/N: 22.78002.011  
Thickness: max 2.2mm (含mylar及螺孔高)  
  
Vendor: FOXCONN  
P/N: 22.78006.011  
Thickness: 2.0mm (含mylar)



Vendor: LOTES  
P/N: 22.78005.171  
  
Vendor: FOXCONN  
P/N: 22.78005.161

HeatSink+FAN Symbol



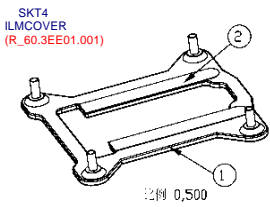
Vendor  
P/N:

Wire Length: 30mm  
  
Vendor  
P/N:  
23.21221.024  
23.21212.031

LABEL



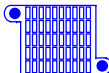
MB serial NO# and MAC address  
40.3KP03.011-> 35 x 15mm  
40.3BZ24.011-> 30X15mm  
45.41107.021-> 70 x 8mm  
40.3BZ23.001-> 30\*10mm  
40.3BZ23.011 >30\*10



Vendor: LOTES  
P/N: 22.78005.171  
  
Vendor: FOXCONN  
P/N: 22.78005.161

34.3KF01.001 for 5.2mm slot 62.10043.G11  
34.3HJ03.001 for 9.0mm slot 62.10043.E41

HeatSink Symbol



HS10  
HEATSINK  
(R\_60.3ET05.001)

Vendor  
P/N:  
60.3ET05.001  
60.3ET05.011  
60.3ET05.021



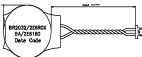
GSKT1  
GASKET  
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Battery Symbol



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BATTERY CR2032  
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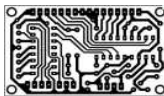
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23.20023.311  
23.22063.001



BAT2  
BATTERY BR2032\_60MM  
(R\_23.24220.612)  
Wire Length: 60mm  
耐高溫>85C

Vendor  
P/N:  
23.21208.061  
23.24220.612

PCB Symbol

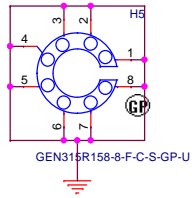
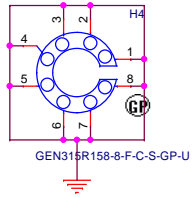
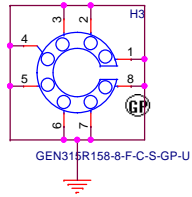
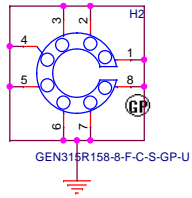
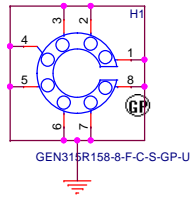


PCB1  
PCB

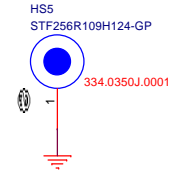
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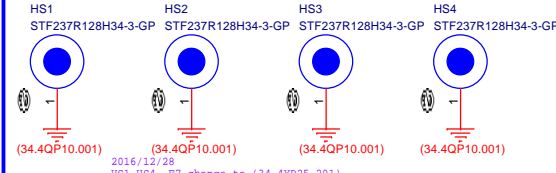
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
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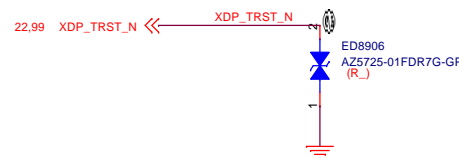
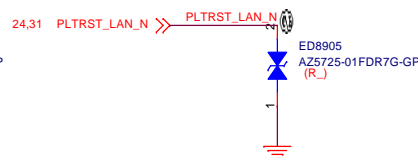
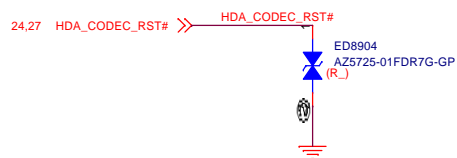
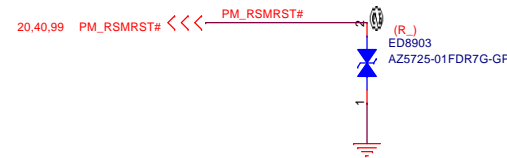
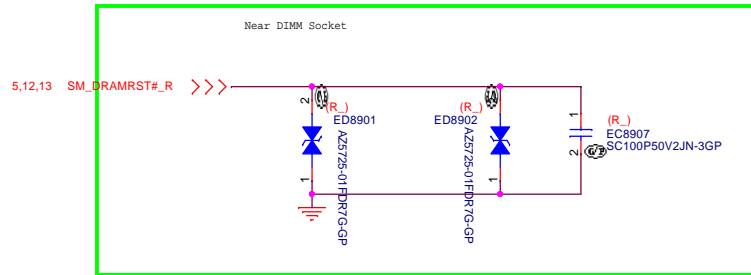
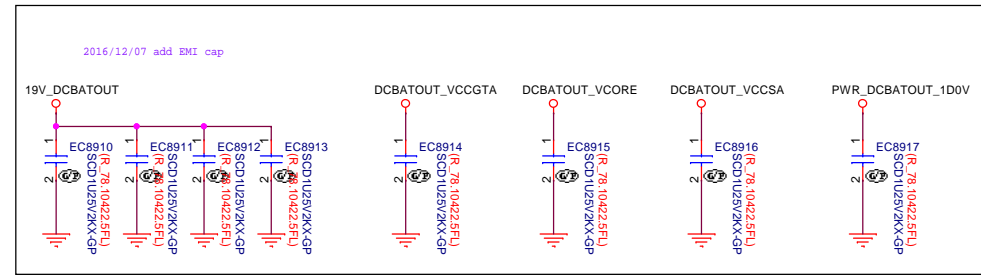
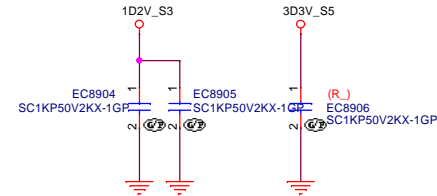
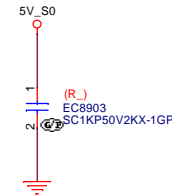
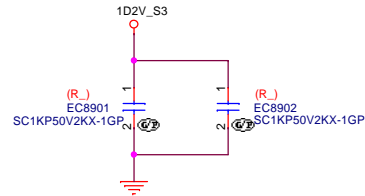
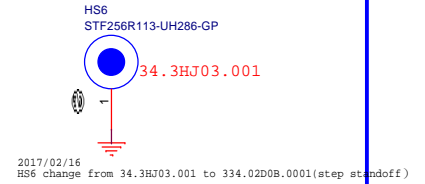
## WLAN (M2 key E)



## CPU



## SSD (M2 key B)



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Title <b>RSVD</b>			
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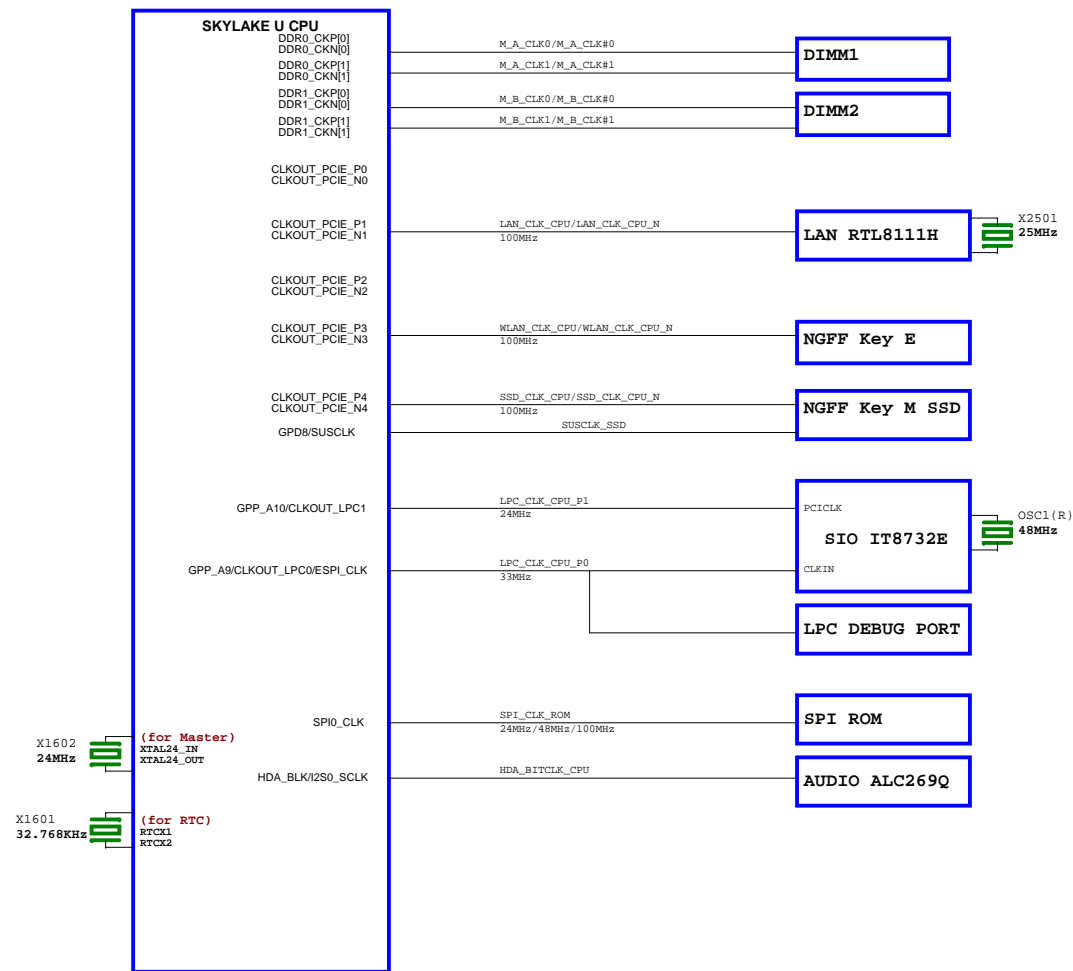
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Title <b>XDP</b>			
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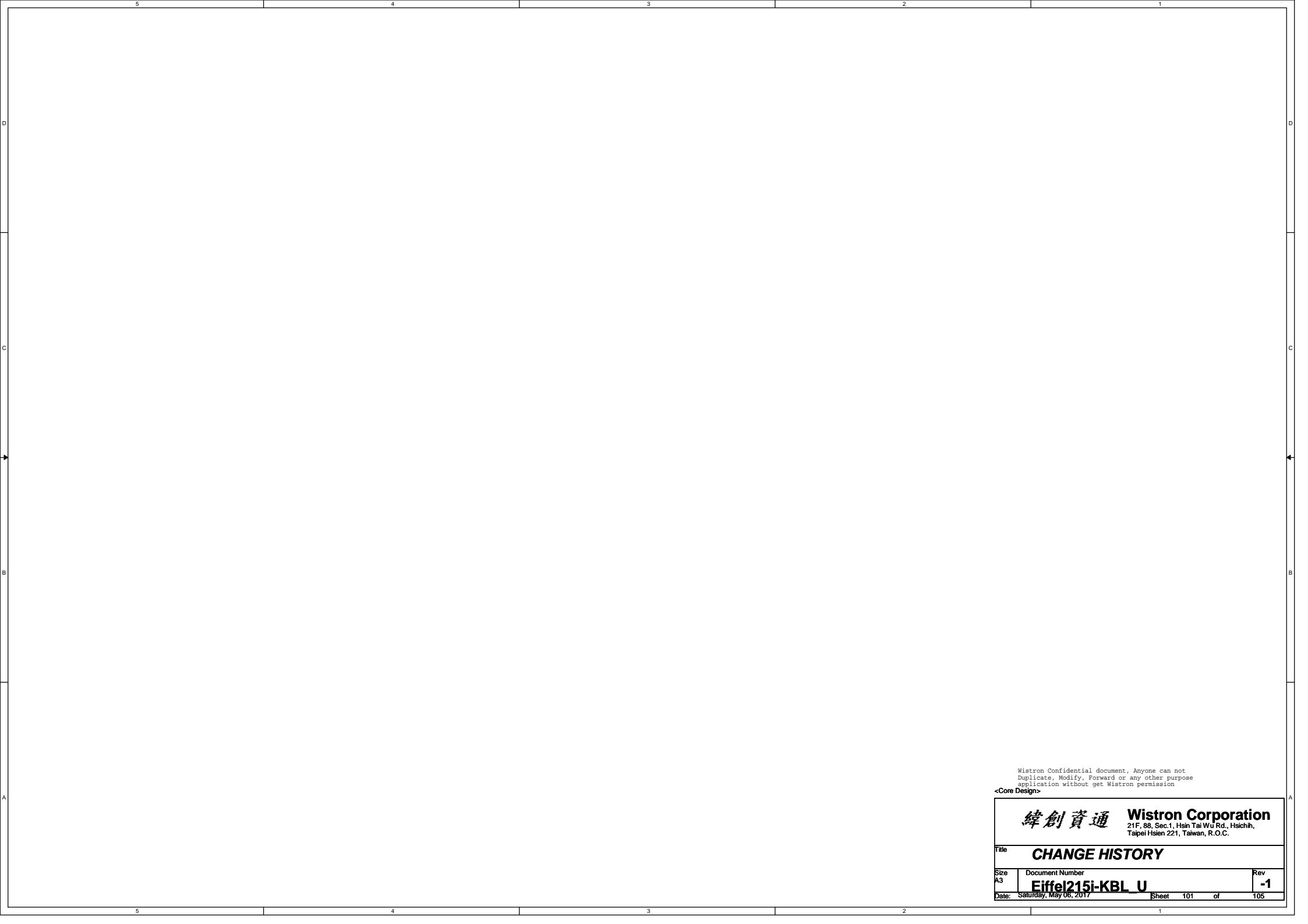
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Title <div>TABLE OF CONTENT</div>		
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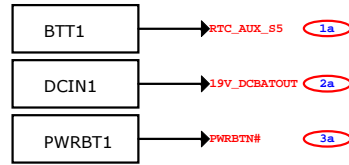


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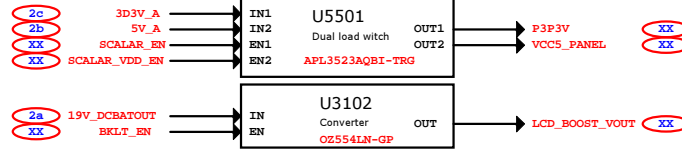
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TitleCHANGE HISTORY	
SizeA3	Document NumberEiffel215i-KBL U
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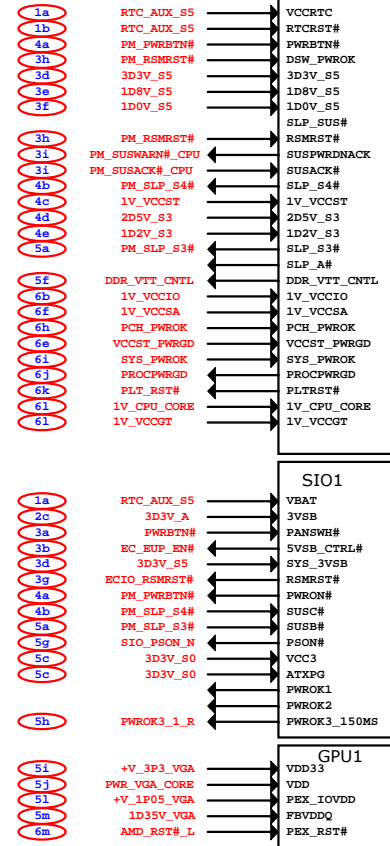
## External Events



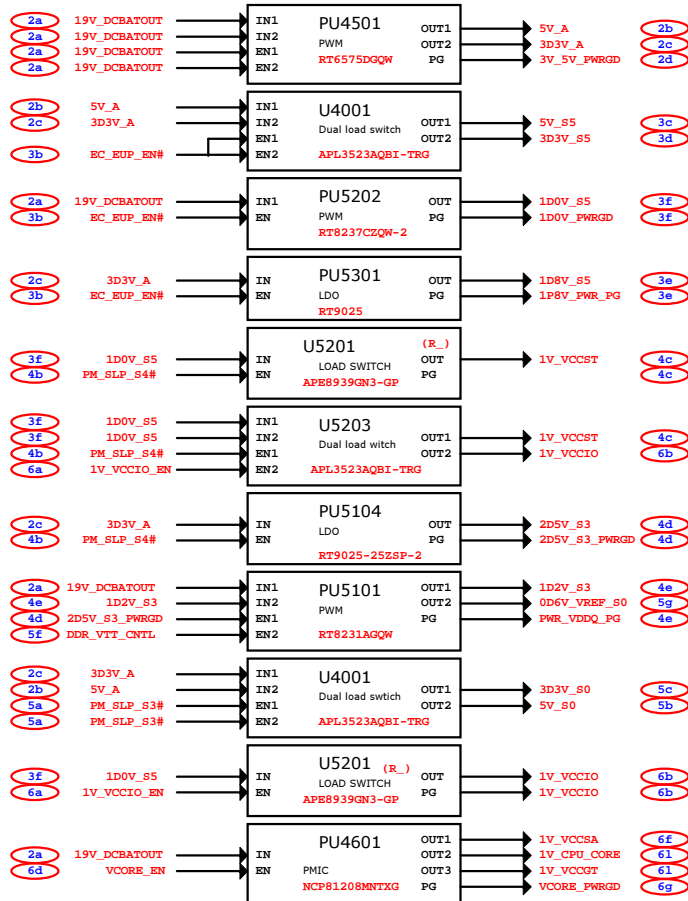
## Panel Powers



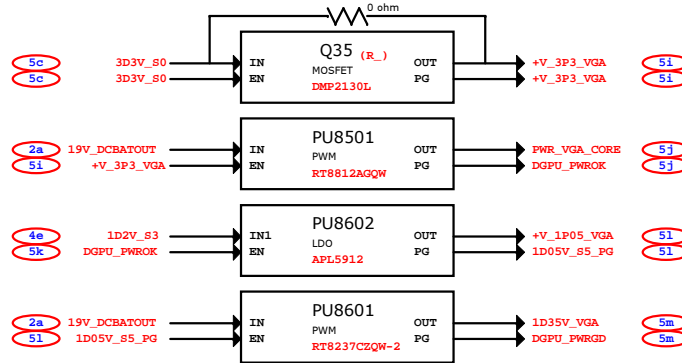
## Chipsets



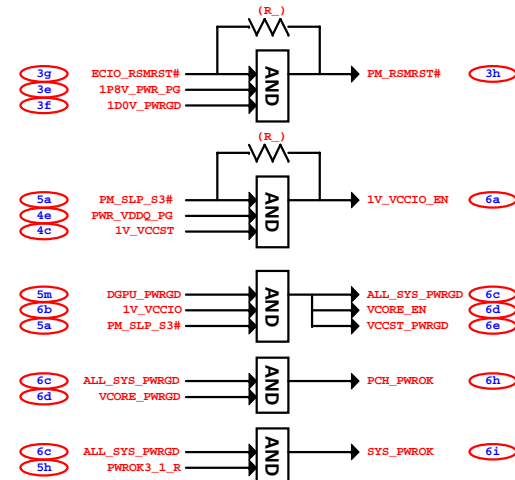
## System and CPU Powers



## GPU Powers

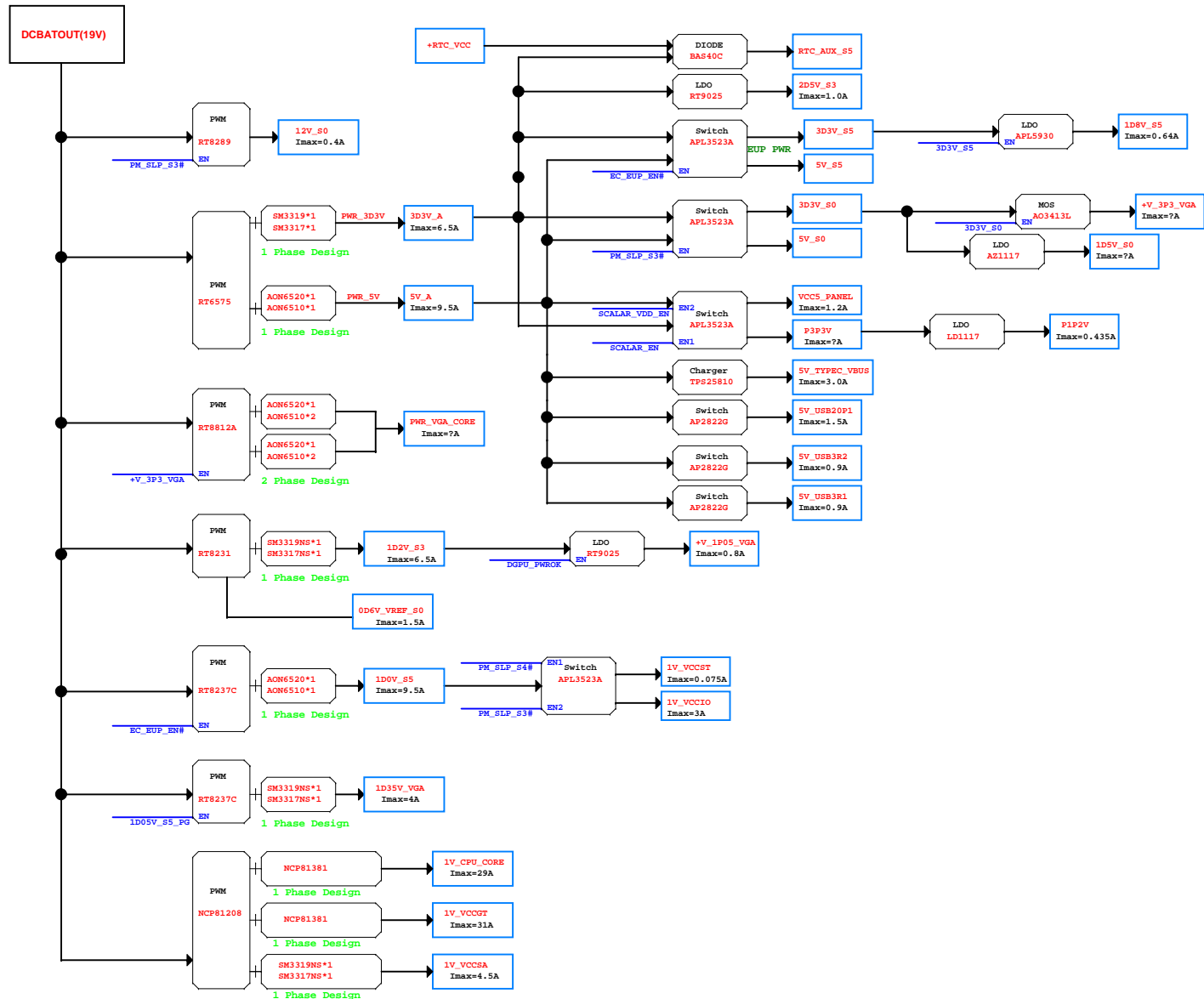


## Power Sequencing

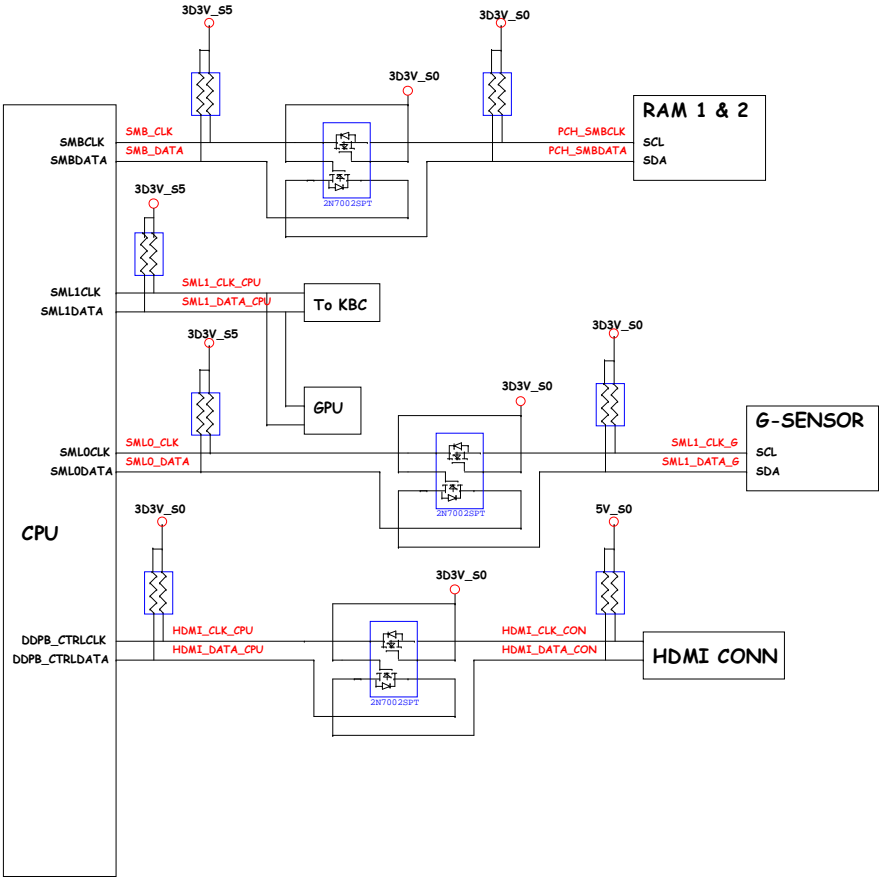


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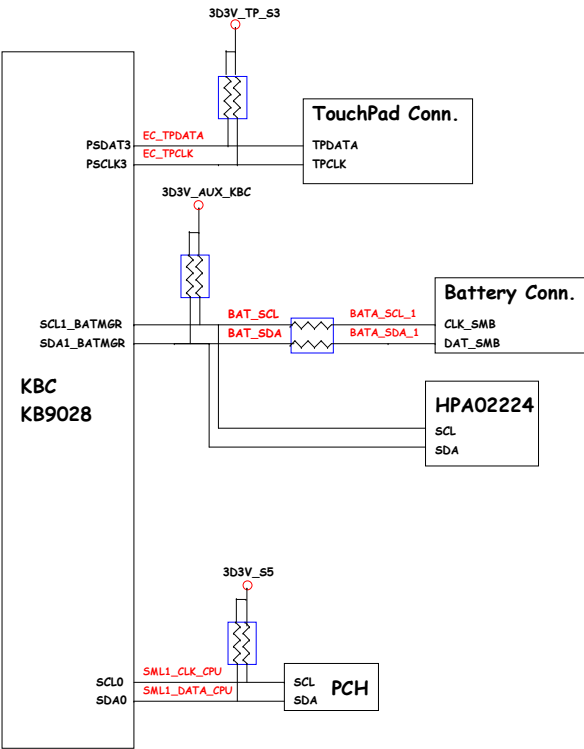
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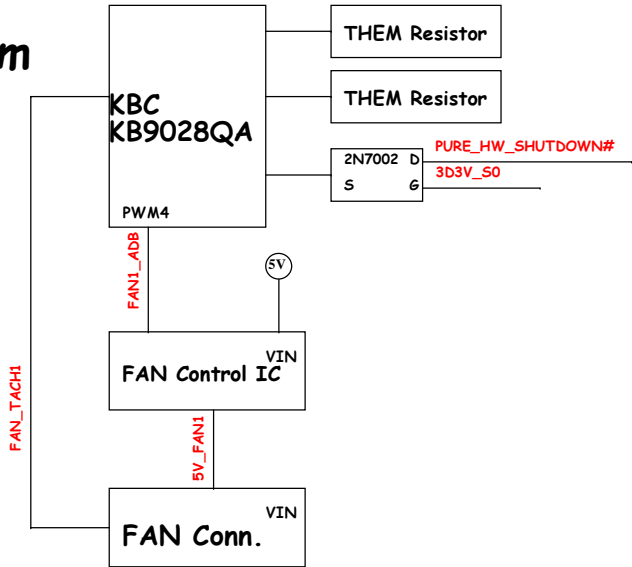
PCH SMBus Block Diagram



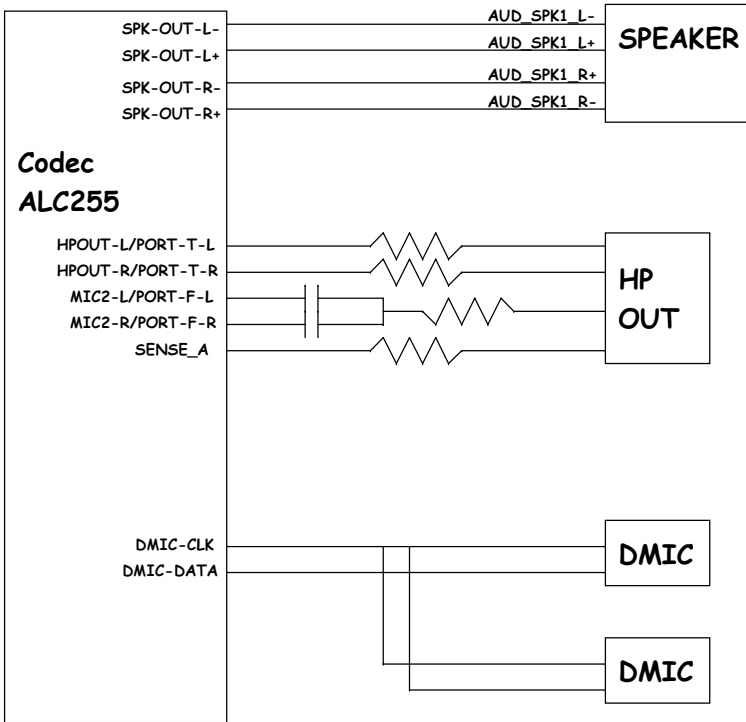
KBC SMBus Block Diagram



# Thermal Block Diagram



# Audio Block Diagram



# System Reset



# PROCHOT Mechanism

